

Design and Implementation of Digital Electronics for Fast Readout and Processing of Multi-Channel Experimental Data

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Synopsis

InnoSys, Inc. and the University of Hawaii (UH) Instrumentation Development Lab (IDL) have been developing prototype hardware and related firmware and software for STRAP: Scalable Triggering, Readout and Processing unit for next generation data acquisition systems to be used in NP experiments and applications.



Some Background on InnoSys



Some Background on InnoSys

- Founded in October 2000.
- Small business focusing on supporting customers with their system specific needs including those involving high temperature, harsh environments, radiation hard electronics.
- Manufacturing Solid State Vacuum Device (SSVD™) TWTs, TWTAs, high temperature and harsh environment vacuum and radiation hard/insensitive electronics.
- 32,000-square-foot facility in Salt Lake City, Utah.
- Capability
 - Microfabrication facility and process
 - Class 100 cleanroom for photolithography
 - Class 1000 cleanroom for process
 - Testing - complete DC, high frequency (DC to greater than 140 GHz), and optical measurements.
 - Characterization – including electrical characterization, scanning electron microscope (SEM) and optical microscopes.
 - Assembly and packaging facility
 - Device simulation and computer aided design (CAD) capability which includes electromagnetic, thermal, structural analyses based on both commercial and internally developed software.
 - In-house mask making - for fast turn around development cycles



Some Background on InnoSys

- Complete in-house machining, vacuum electronics assembly and packaging manufacturing capability.
- Integrated 3-dimensional computer aided design (CAD)/mechanical modelling and simulation and vacuum electronic device modelling and simulation capability.
- Strong capabilities in integrated circuit including application specific integrated circuits.
- Design, implementation and manufacturing of printed circuit board based electronics including power supplies, drivers, controllers, sensors, etc. for lighting, communications, high voltage power supplies, high speed data communications, wireless control and communications, etc.



Examples of InnoSys Facilities



I
C
D
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N



Cleanrooms for MEMS and
Microelectronics, Micromaching, etc.

DOE-NP SBIR/STTR Exchange Meeting August 8-9, 2017 Gaithersburg, Maryland

InnoSys Product Families

In addition to High Frequency and High Power Amplifiers and Electronics and Harsh Environment Electronics, InnoSys also has commercial solid state lighting products (iLumens by InnoSys) including LED lamps, LED fluorescent lamp replacements, lighting controls and sensors (see following pages)

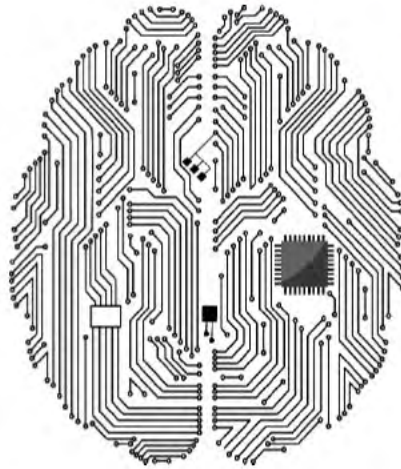
iLUMENS™

BY INNOSYS

InnoSys makes LED Lamp “Brains” as well as the LED Lamps

We make these

Hardware
Firmware
Software



for these



One of iLumens by InnoSys Datasheets

One of InnoSys' iLumens by InnoSys Product Datasheet

This product is in Commercial Mass Production and is sold to Commercial, Industrial, Government, and other End Users.

iLumens
by InnoSys

Part Name: Ally Lamp
Part Number: LT84-4000-BWR-1620

Easily Turning Fluorescent Fixtures into an Intelligent LED Platform

Features and Benefits

- Plug-and-Play** installation means less retrofit costs and saved time. The lamps are compatible with most electronic ballasts.
- Dimmable** lamps (0-100%) that work with a traditional ballast. In place significantly improve system efficiency and user comfort.
- Constant Lumens** current-control technology means equal lamp brightness, regardless of ballast model, helping with aesthetics, lamp lifetime consistency, and energy performance.
- Compatible** with 0-10V smart controls and sensors (daylight, occupancy, etc.), allowing flexible integration with the lamps.
- Advanced Efficiency** from modern LEDs, sensors, and smart controls means up to 85% energy savings over linear fluorescent lighting.

Description

iLumens turns your existing fluorescent lighting infrastructure into an intelligent lighting system. Ballast-compatible dimmability eliminates the need for ballast removal and enables far more energy savings than the 50% saved from LEDs alone (e.g., 85%). The iLumens Ally lamp works with others: 0-10V controls, sensors, and software, providing advanced energy savings and user comfort. With high-performance and economics in mind, iLumens is the optimal method for achieving intelligent LED lighting in a linear fluorescent space.

Awards

- Winner: *Utah Innovation Award for Cleantech*
- Semi-Finalist: *National Cleantech Open*
- Finalist: *NREL Industry Growth Forum, E2C, SXSW Eco, Next Step Challenge, and Defense Innovation Showcase*

Certifications:

Product Information

Ballast Compatibility: Instant start: >97%
 rapid/programmed start: ~50%
 not designed for magnetic
 Dimming Control: ... 0-10V wired (~1 mA/lamp)
 Correlated Color Temperature (Nom): ... 4000K
 Optics: frosted polymer
 View Angle: 120°

Power: <16W (dimmable)
 Color Rendering Index: ~84%
 Lumen Output: 2079 lumens (dimmable)
 Efficacy: 133 lumens/W
 Lifetime Rating (L₅₀): ... 50,000 hours; longer if dimmed
 Lamp Weight and Dimensions: 0.6 lbs
 47.17 in. 1.11 in.

Photometric Diagrams

Polar Luminous Intensity

Illuminance Cone

Height (m)	Beam Diameter (m)
1.219 m	4.10
2.0 m	6.22
3.0 m	10.09
4.0 m	13.65
5.0 m	16.82

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Technical Intro

For the DOE STTR project we have designed and built prototype hardware that can be used in fast, flexible, scalable and affordable readout and processing systems to maximize the scientific return of current and future Nuclear Physics (NP) experiments.

Coupled with a portfolio of front-end analog electronics, this digital platform is intended to serve as a turnkey solution ready to be deployed in experiments.

Specifically, through the course of this project, InnoSys and UH has designed hardware (HW), firmware (FW) and software (SW), evaluation kits and support for physicists who would like to apply digital signal processing (DSP) and feature extraction techniques to the waveform output of a range of fast sampling ASICs and analog to digital converters (ADCs) within their existing and future experiment-specific DAQ systems.

Examples of Intended Users

Detectors for Internally Reflected Cherenkov light (DIRC),

Electron-Ion Collider (EIC),

Hawaii Muon,

and societal uses such as time-of-flight (TOF) Positron Emission Tomography (PET).

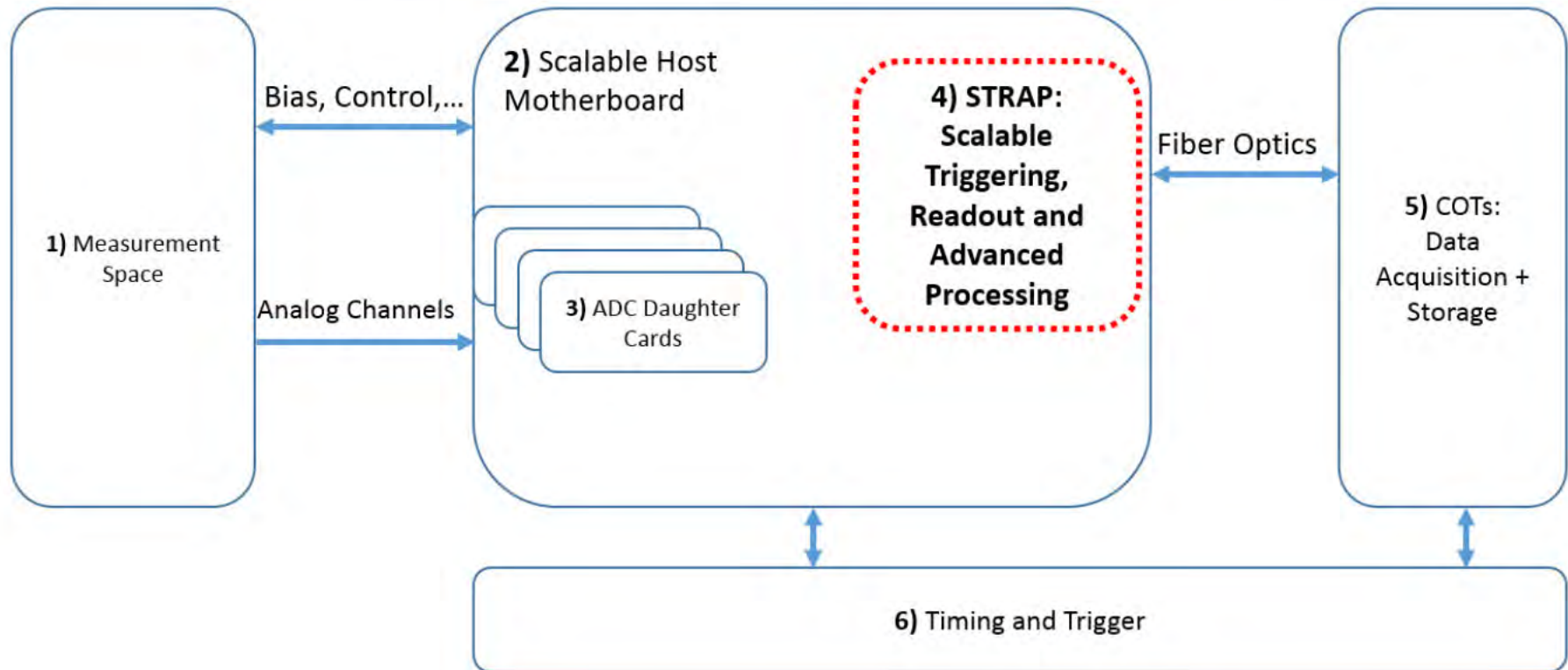
Overall Requirements and Purpose

Such NP experiments require fast and simultaneous processing on up to several hundred channels of detector data per processing node.

A scalable and well maintained readout and processing unit is needed for real time signal processing, feature extraction and data reduction. The output of such a system is then used to create event specific triggering commands and also is recorded to storage media for secondary processing.



Example of Where STRAP Fits In



Electronics setup for a modern Nuclear Physics experiment shown with these elements: 1) Measurement space, 2) A scalable host motherboard, 3) Analog to digital conversion chips and supporting electronics on their respective daughter cards, 4) Digital readout and control system (also the main focus of this proposal), 5) Commercial Off The Shelf Data acquisition and storage, and 6) Timing and trigger.

Current Needs and Our Solution

Need for state of the art DSP circuitry for NP experiments, we are designing and implementing digital integrated circuits and electronics capable of acquiring data from tens to hundreds of fast multi-channel waveform sampling ADCs.

The fast DSP electronics will improve the accuracy in determining the position of interaction points to an accuracy smaller than the size of the detector segments (typically $<100\text{ps}$).

We use digital electronics to create and control trigger based events driving various types of low power waveform sampling ADCs and perform real-time DSP and feature extraction operation on the digitized waveform.

Proposed Design/Solution

Our proposed design/solution will substantially reduce cabling complexity through increased integration and will make the design suitable for installation in experiment or detector chambers.

Installation within the detector will require meeting strict heat generation for electronics, which can be mitigated by a low power design.

Our design is a highly scalable and integrated.

Power/performance trade-off is available through firmware and software customization.



Architecture of the STRAP Design

The next slide shows a block diagram of the STRAP, a single all digital board design, which comprises of an FPGA, RAM, clock and fiber optics transceivers. The connectors on the board allow it to be connected to a variety of motherboards and waveform sampling ASICs/ADCs.

The board also provides connectors for communications with a Gb Ethernet network and also a main clock and trigger system which will be applicable to systems with multiple STRAPs.

Features of this design at a glance include:

Hardware with expanded firmware and software development kit (FDK, SDK)

Compact form factor: 4"x2.6"

FPGA: Xilinx Artix-7

HPC FMC with ~300 fast digital IOs

Calibration SRAM: 4MB onboard

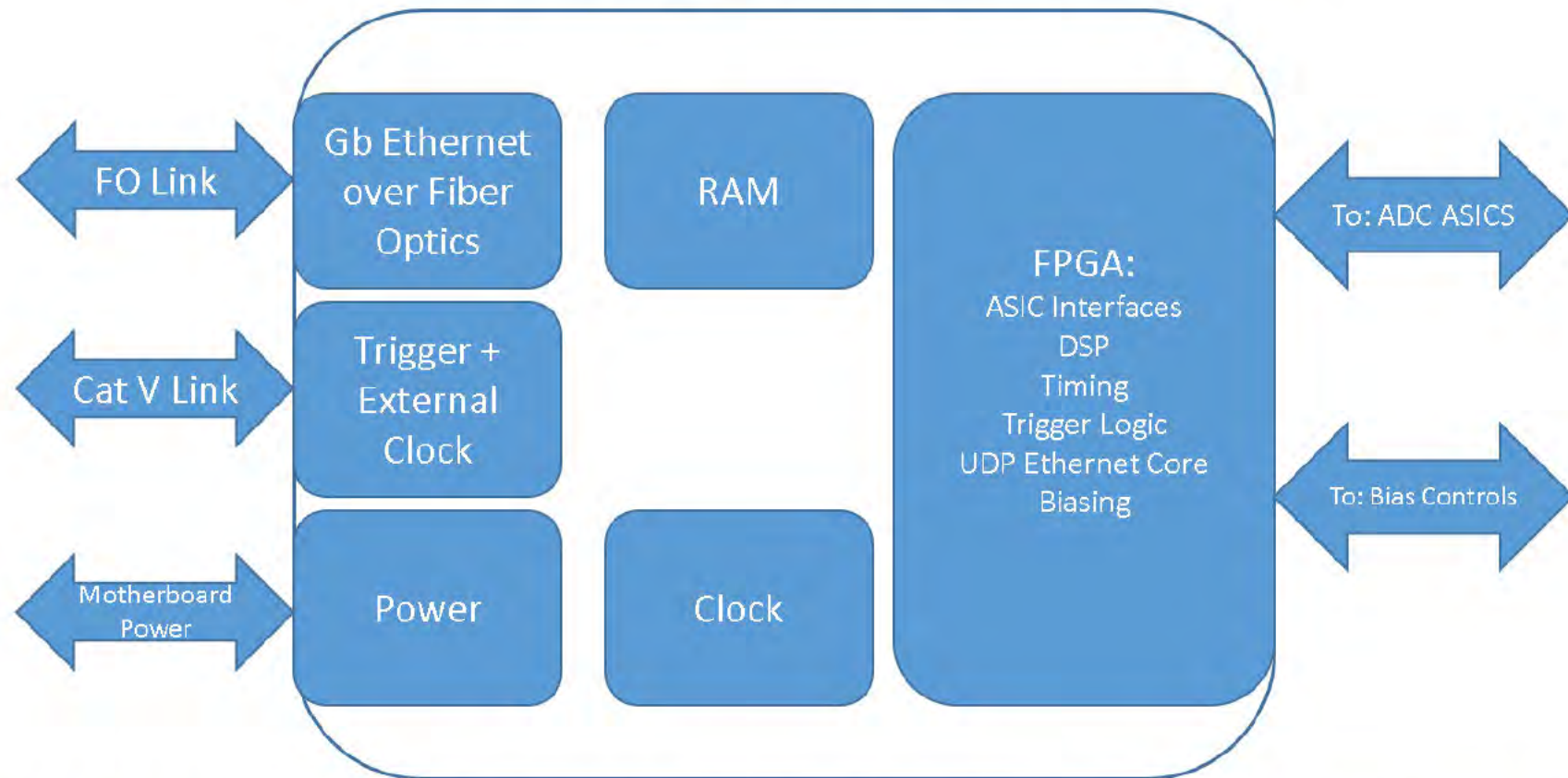
4+Gbps optical transceiver with optional user diagram protocol (UDP)

Firmware and software development kits

Built-in compatibility with various fast ASICs: IRSX, TARGETX, PSEC4, HalfGRAPH

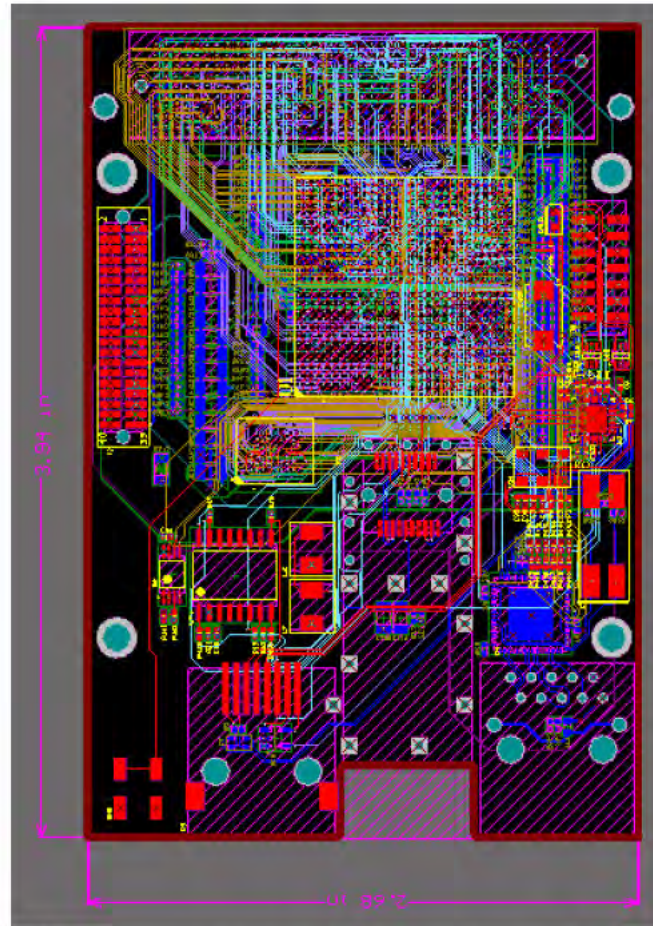
Supports ~100s of front end analog channels

Block diagram of STRAP



The block diagram of the STRAP, a single all digital board design is comprised of an FPGA, RAM, clock and fiber optics transceivers. Connectors on the board allow use of a variety of motherboards and waveform sampling ASICs/ADCs. The board also provides connectors for communications with a Gb Ethernet network and also a main clock & trigger system which is applicable to systems with multiple STRAPs.

STRAP Prototype Version 1



(Left) A photo of the top view of the first version of the actual STRAP board with the high density pin connector not soldered on and (Right), the routed PCB layout- top layer of the PCB. Note there are numerous components on the 'back side' of the PCB

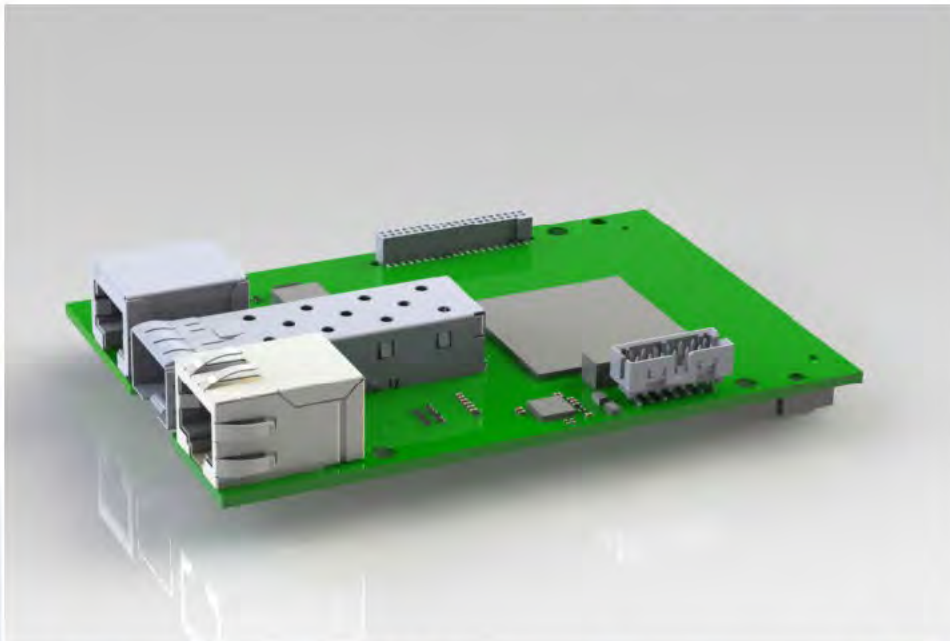
Mechanical Considerations

A High Pin Count FMC (HPC-FMC) connector that provides over 400 high speed IO pins.

This FMC connector will carry both power and high speed Low Voltage Differential Signals (LVDS) to and from the analog frontend chips.

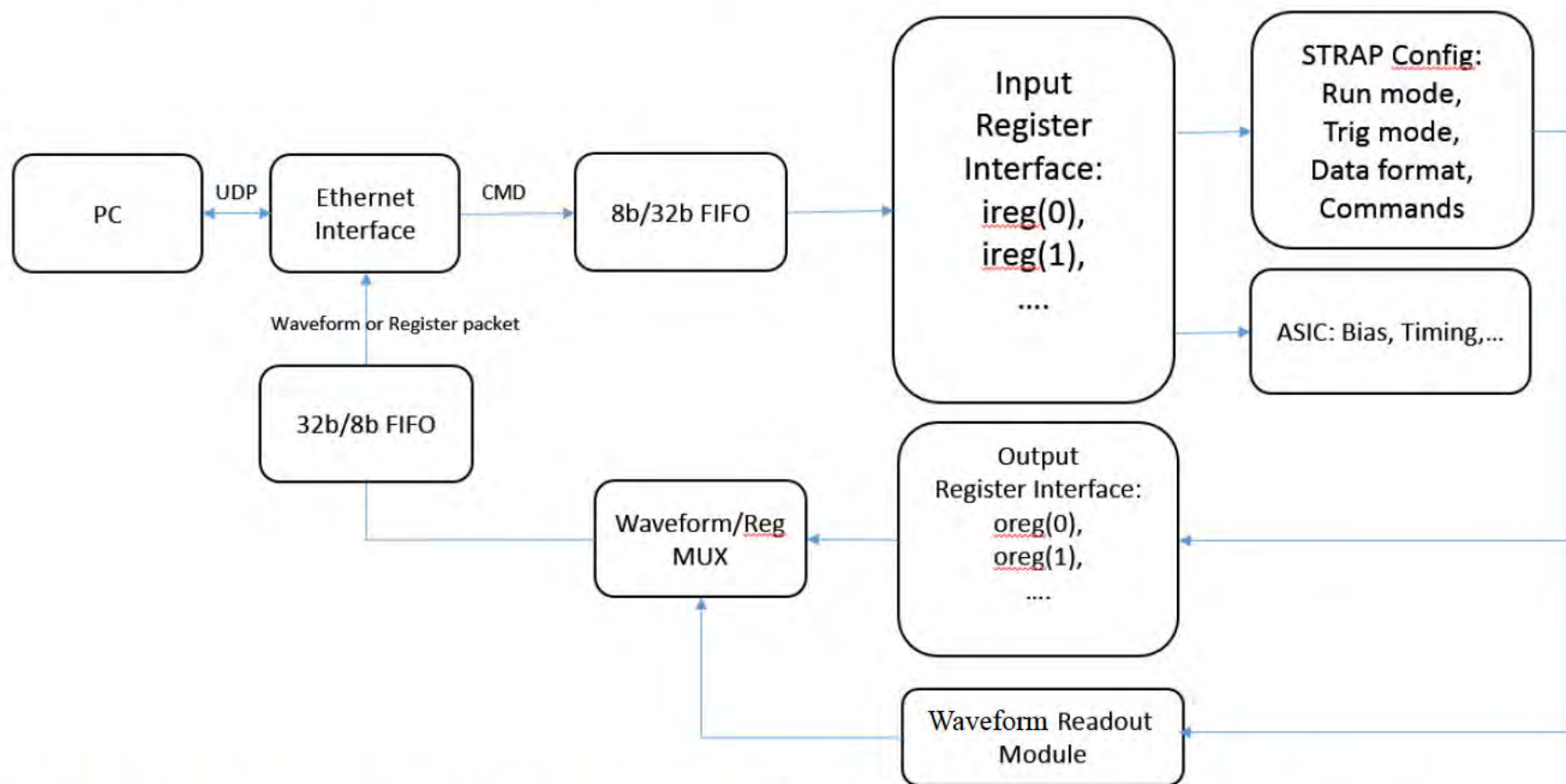
Given the density of the pins and tight spacing, the routing is a complicated task in this case, for which several iterations were performed to gain and obtain optimum results.

Design and Reality



(Left) A 3D rendering of the Version 1 STRAP board and (Right) a photo of an actual manufactured unit. The STRAP printed circuit board (PCB) is 12 layers.

Firmware Overview for STRAP



In order for the board's FPGA to be able to perform the desired functions, we need to program it with a specific firmware (FW). This FW is responsible for communicating both with the FPGA and the frontend electronics (Hardware) and the outside world (Software).

We designed and implemented custom FW using the leading industry standard Vivado tool offered by Xilinx. Figure 4 shows the components of the FW. As seen in the figure, there are several modules involved in the operation of the FW. The key components are the UDP communications block, the command interface with the list of registers, and the ASIC/frontend control block.

Firmware overview for STRAP

The FW common platform is related to the general STRAP operation and includes the communications with the host and also a command interface.

This modular design ensures possibilities for future expansion, backwards compatibility and also code's reusability for next generation and commercialization efforts.

Additionally, FW is being designed with a Firmware Development Kit (FDK) approach.

The STRAP can be used as a test-bed for prototyping more complex experiments and identifying the best FW/SW needs and capabilities for a special case.

In generating this FDK we have considered, among other things, the following:

Modular design.

Code hardening to minimize the need to know internal operations of the each block.

We plan add extra features such as example designs to accelerate end-user acceptance and lower the barrier to adopt the STRAP technology.

Software Design

The Universal Datagram Protocol (UDP) approach for the software design will ship with mainstream operating systems such as Windows, Linux or MacOS.

For rapid prototyping we created code in Python, where the code is capable of sending commands to the STRAP module via the UDP interface and read back status packets from the STRAP.

Each STRAP has a unique IP address which will make it easy to identify multiple STRAPs on the same interface and communicate with them.

The command packets sent to the STRAP will modify the values of an internal set of registers. These registers can control general STRAP operational modes or they can control the analog front end properties.

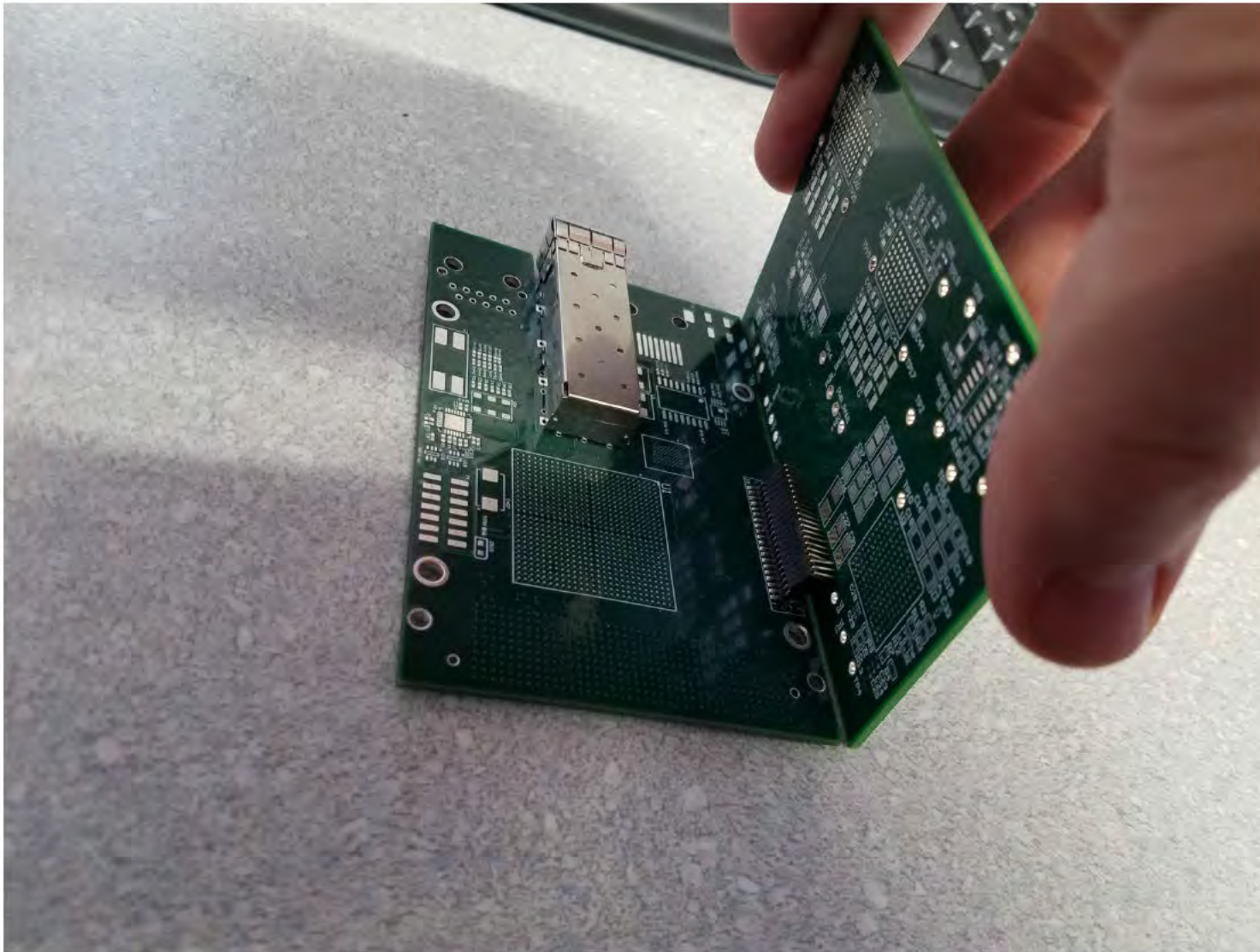
These properties include but are not limited to gain, offset, sampling speed, timing, calibrations and many others specific to the waveform sampling ASIC.

Python, as a widely accepted language for rapid prototyping, was used. For the final product we are planning to use C++ for low level functions where runtime speed and robustness is of an essence.

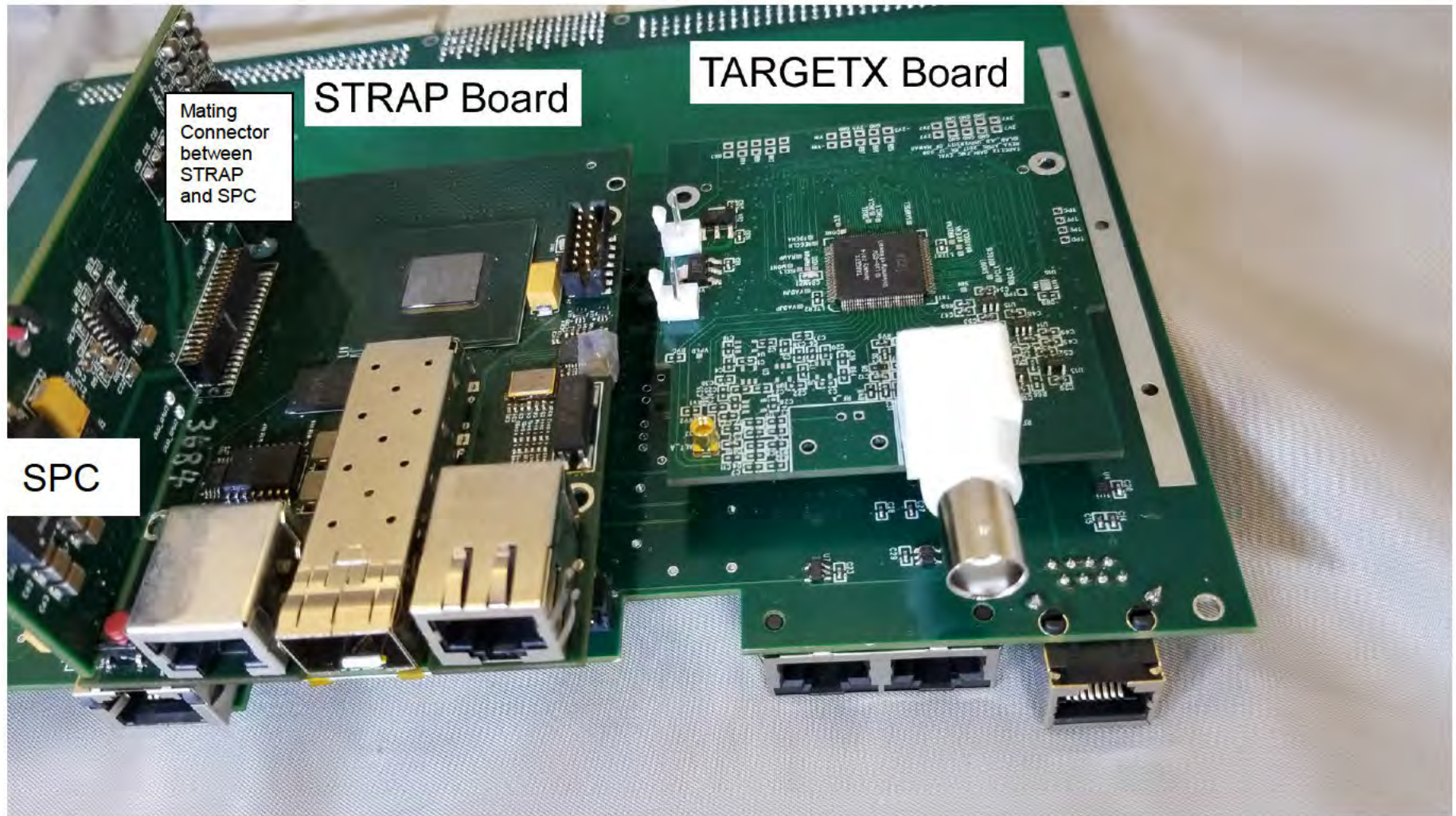
The STRAP Power Conditioner Board

- The FPGA family that is used is a complicated Chipset that requires precise voltages and timing to function properly.
- Therefore we designed several versions of a STRAP Power Conditioner/Timing Board.
- After a couple of iterations we were able to achieve full functionality and form/fit factor.
- An example STRAP Power Conditioner Board is shown in the next slide.

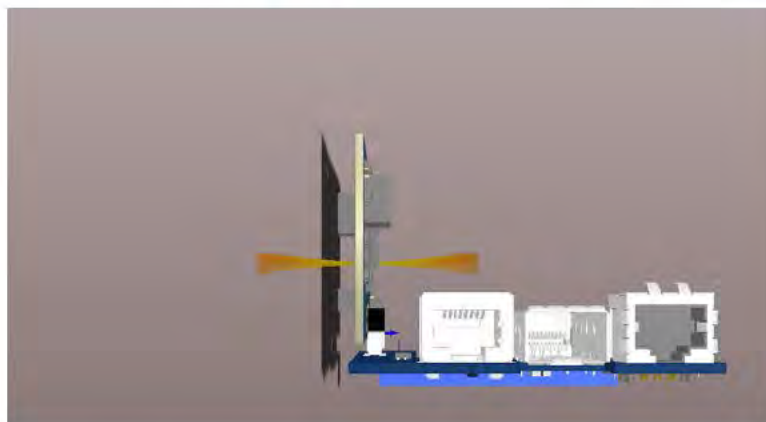
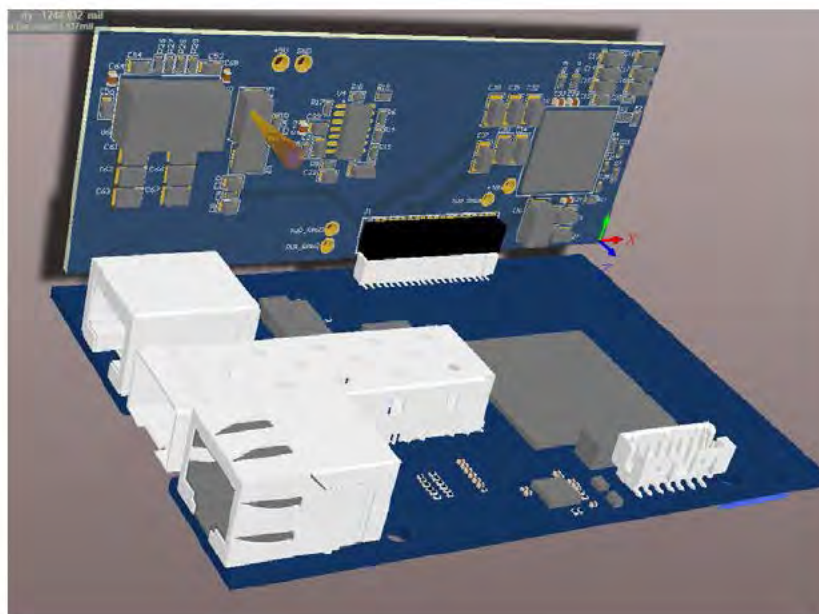
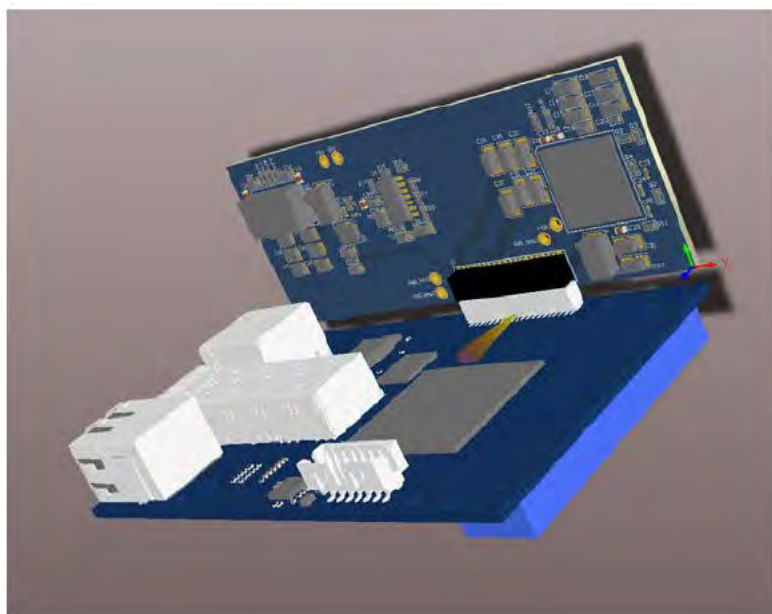
Bare STRAP mounted to Bare STRAP Power Conditioner PCB



Test and Development using a Prototype STRAP with a TARGETX



Renderings of New Version of STRAP Mated to Power Conditioner Board

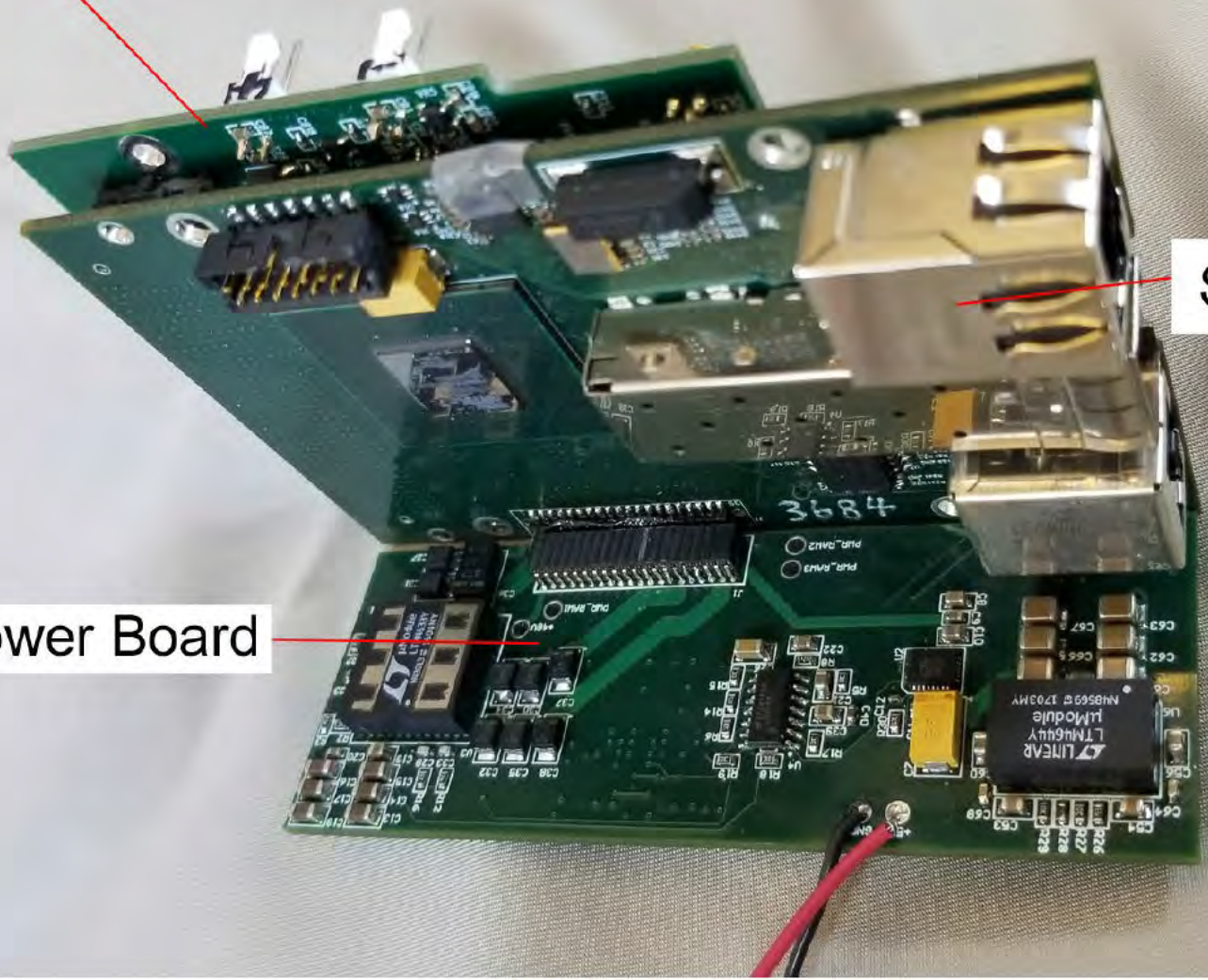


Example of Functional Ver. 1 STRAP

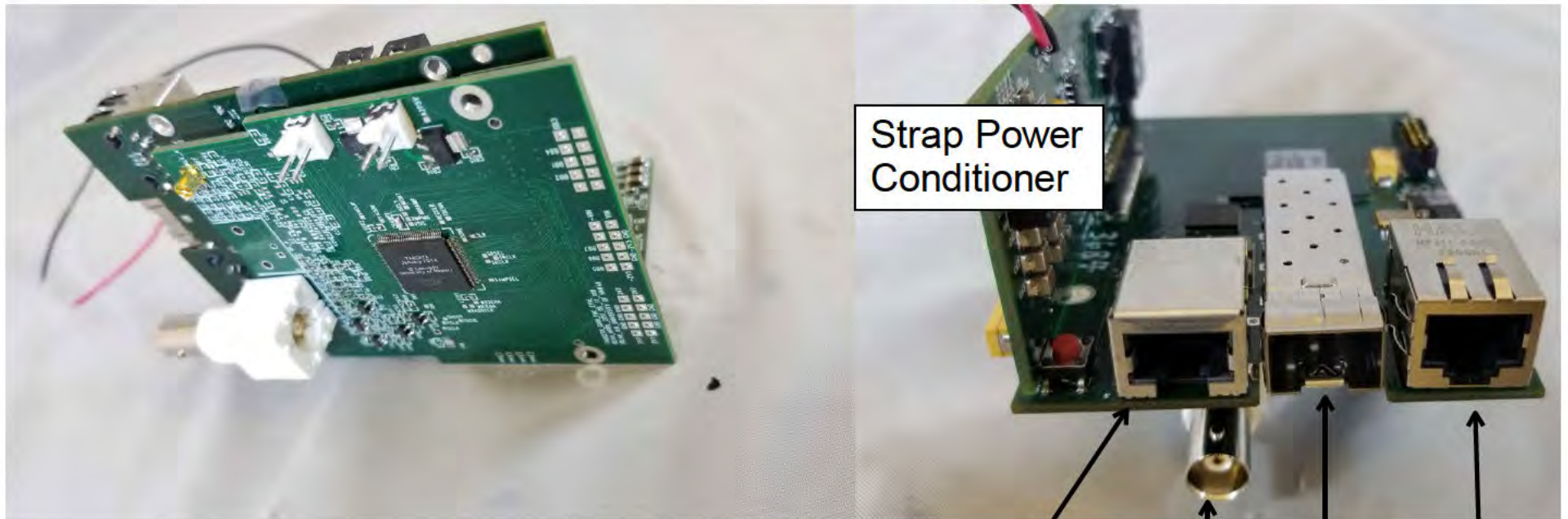
TARGETX Extended Range Board

STRAP

STRAP Power Board



Other views of STRAP and TARGETX Integration



Strap Power Conditioner

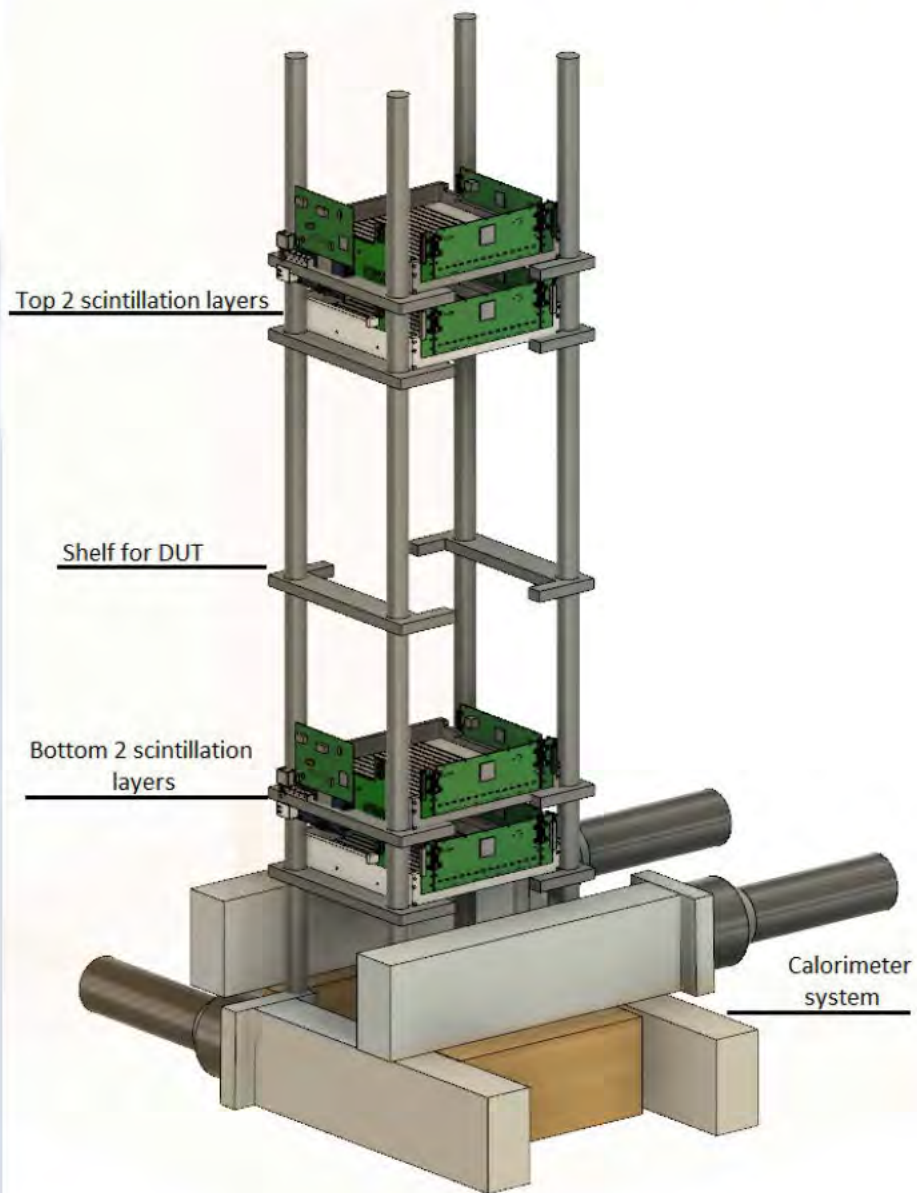
Clock Distribution and Triggering

Detector Pulse Input

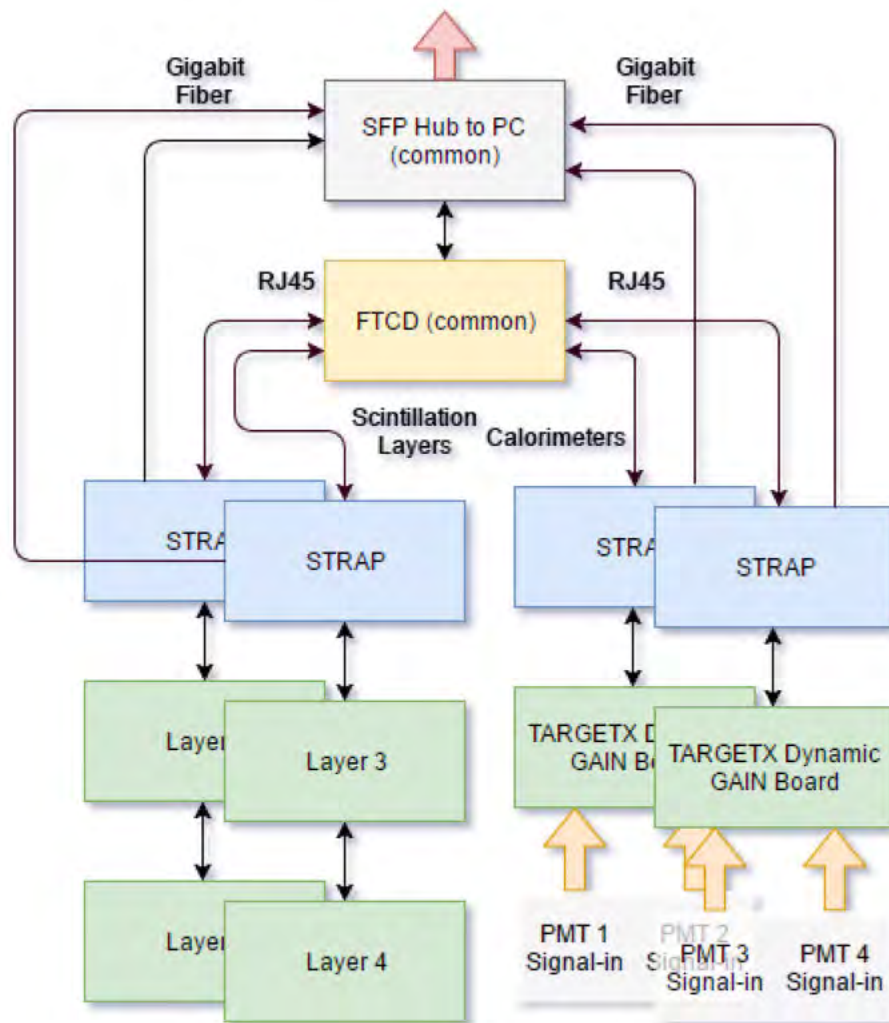
Fiber Data Out

Ethernet Data Out

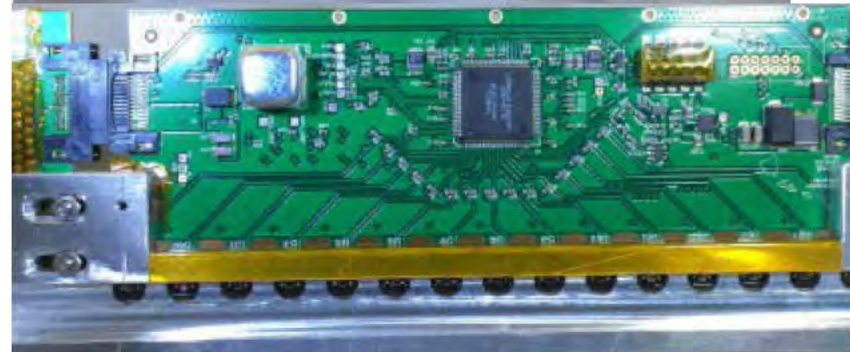
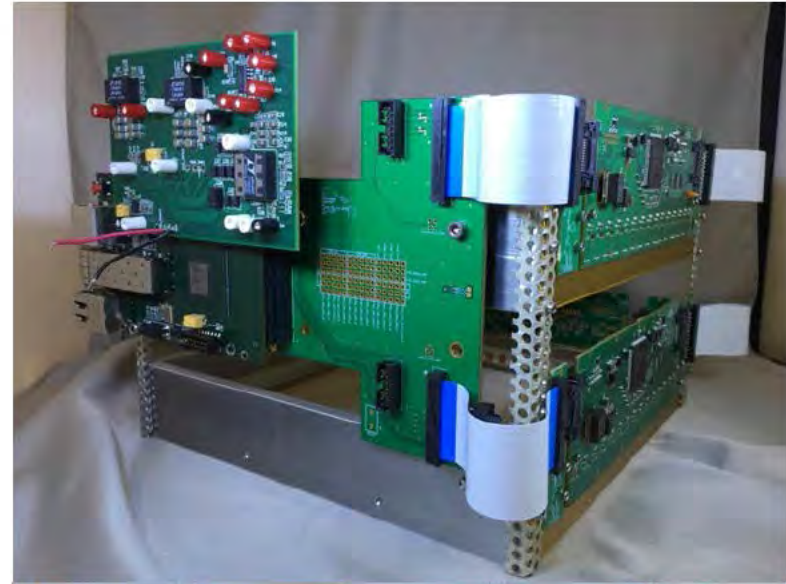
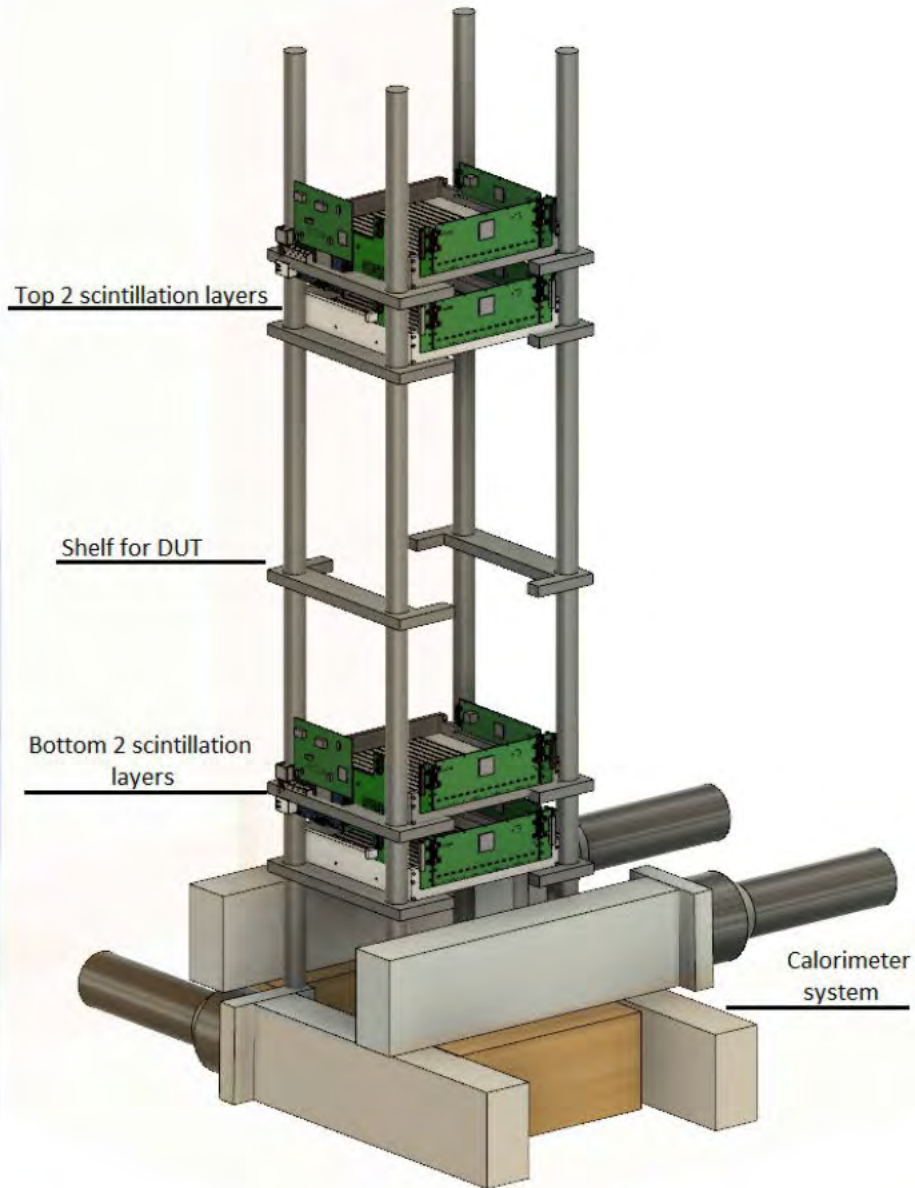
Hawaii Muon Beamline



3rd Generation



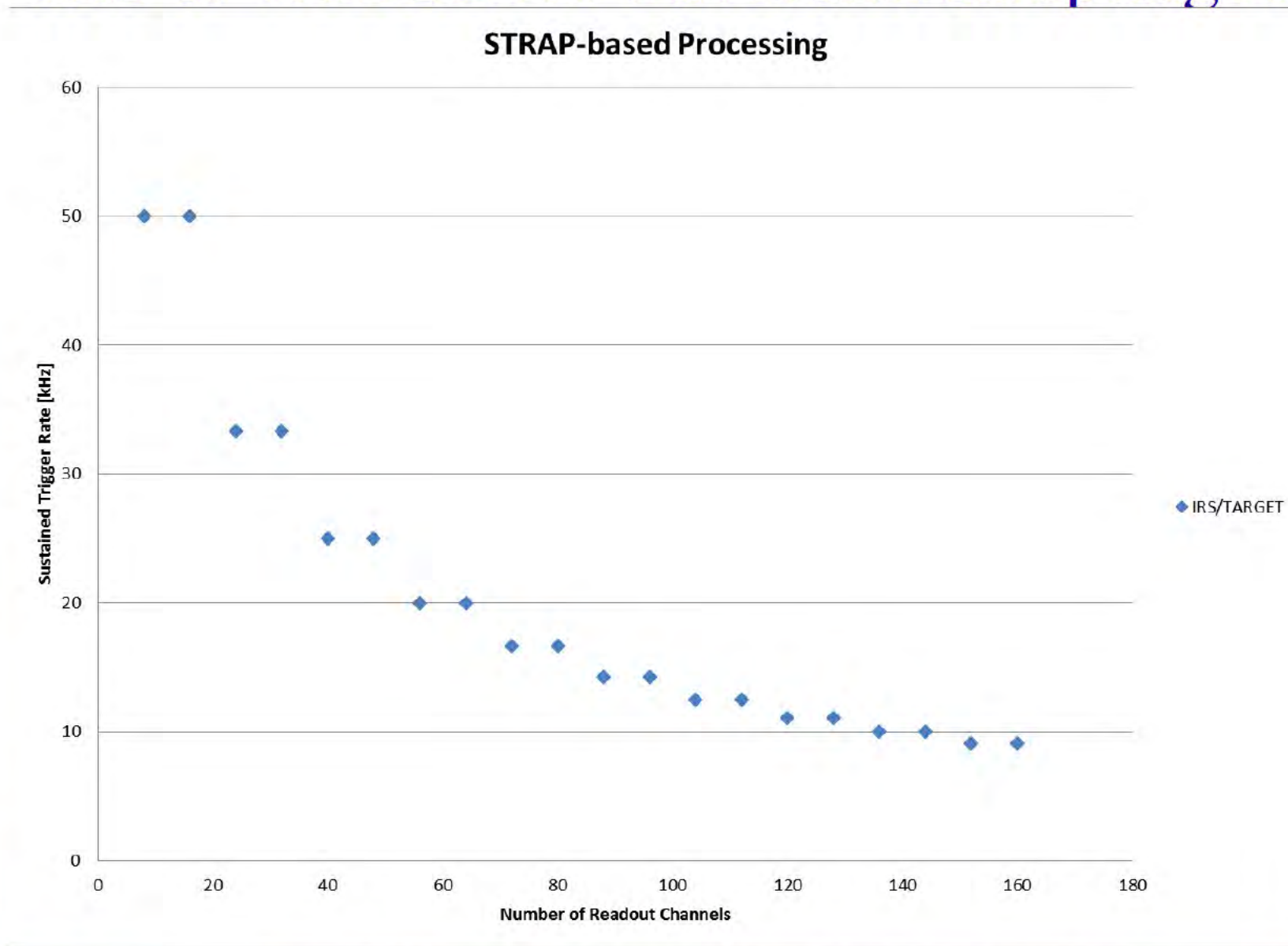
Hawaii Muon Beamline



Thoughts on UTA Muon Detector

- TARGETX readout is well matched to such an application
- For existing 448 channel detector, trim long fibers, add MPPCs/SiPMs at cylinder edge
- 28 TARGETX ASICs
- 28 or 7 TARGETX “daughtercards” (16 or 64 Ch.)
- Single STRAP FPGA processing/ethernet I/F and acquisition from all 448 channels
- Form factor of cards would need change, but bulk of effort in Firmware/Control/DAQ

Processing throughput of STRAP when used with IRS or TARGETX waveform sampling ADCs.



Acknowledgments

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Thank you

Questions?

