ALPHACORE

Analog, Mixed Signal & RF Electronics

Radiation-Tolerant High-Speed Camera

Contract # DE-SC0013232

DOE NP SBIR/STTR Exchange Meeting
August 8-9, 2017
Gaithersburg, MD

Outline

- About Alphacore
- Program info
- Introduction to radiation effects in image sensors
- High-speed camera architecture and first prototype implementation
- Future plans
- Summary

About Alphacore

- Founded in 2012 and located in Tempe, Arizona
- Providing technologies that enable major advances in:
  - Homeland Security
  - Defense
  - Aerospace
  - Scientific Research
  - Medical Imaging

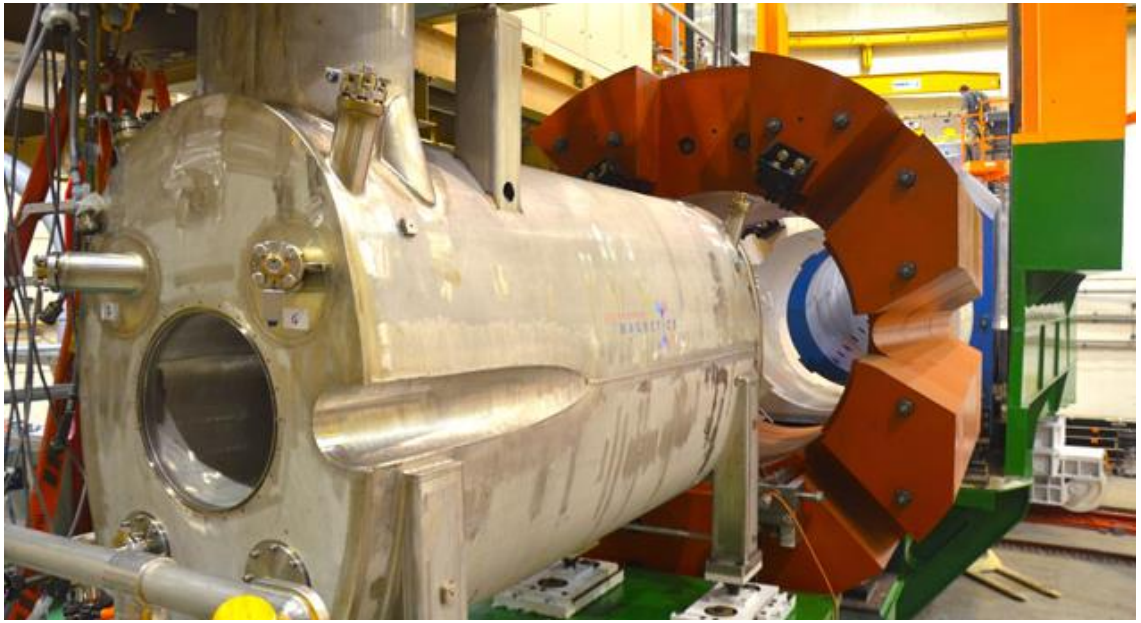
- Product areas span:
  - High performance analog, mixed signal, and RF electronics
  - High-speed visible light and infrared camera systems
- Rapidly Growing

Program Info

DOE SBIR Phase II Contract #DE-SC0013232

DOE need:

A radiation-tolerant, triggerable, **high speed imaging chip and a complete camera system** for investigating rapidly occurring phenomena in radiation environments. The primary applications are beam monitoring and scientific experiments at nuclear physics facilities.



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Motivation

Non-hardened image sensors and cameras typically do not operate beyond few tens of kilorads

Hardened sensors and cameras typically target nuclear plant monitoring applications and have low frame rates (30fps)

High-speed rad-hard image sensors and cameras do not exist (to the best of our knowledge)

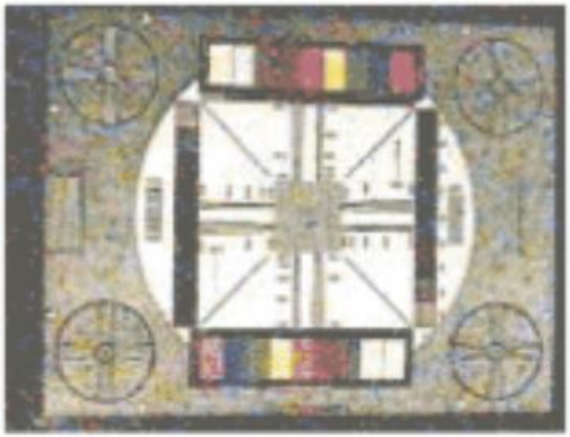
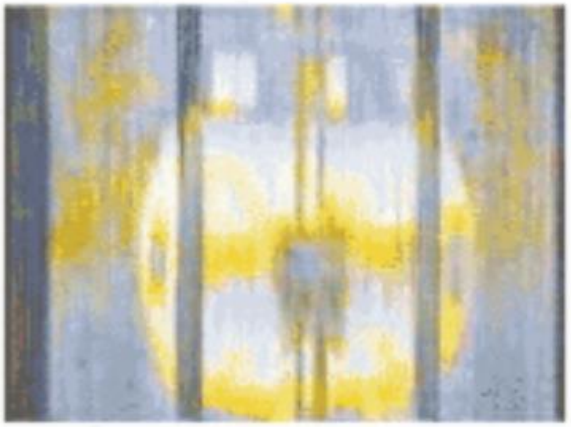


Image before irradiation



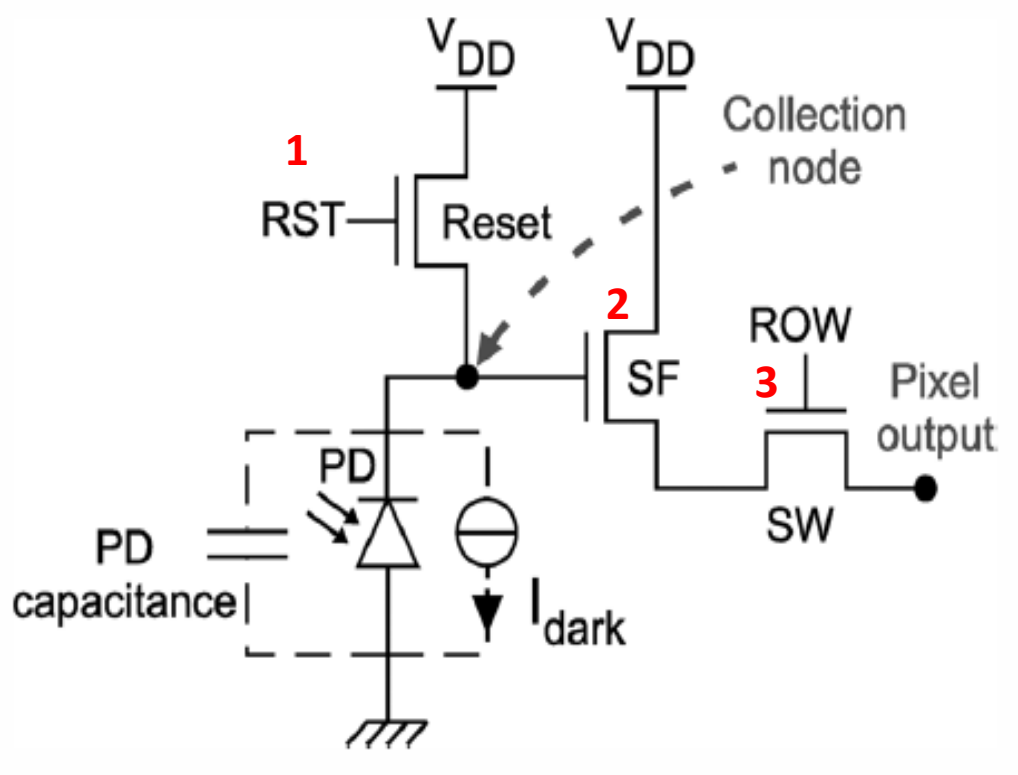
…and after 10krad

[Courtesy: Vision System Design]

Camera Specifications

Specification	Description
Resolution	Minimum: 10 kilopixels Objective: 1 Megapixel
Frame rate	Minimum:1 kfps Objective: 10 kfps
ADC resolution	10 bits *Dynamic range increased with a programmable gain amplifier*
Pixel	20 µm x 20 µm pixel size 65% fill factor
TID tolerance	Minimum: 100 krad Objective: 300 krad

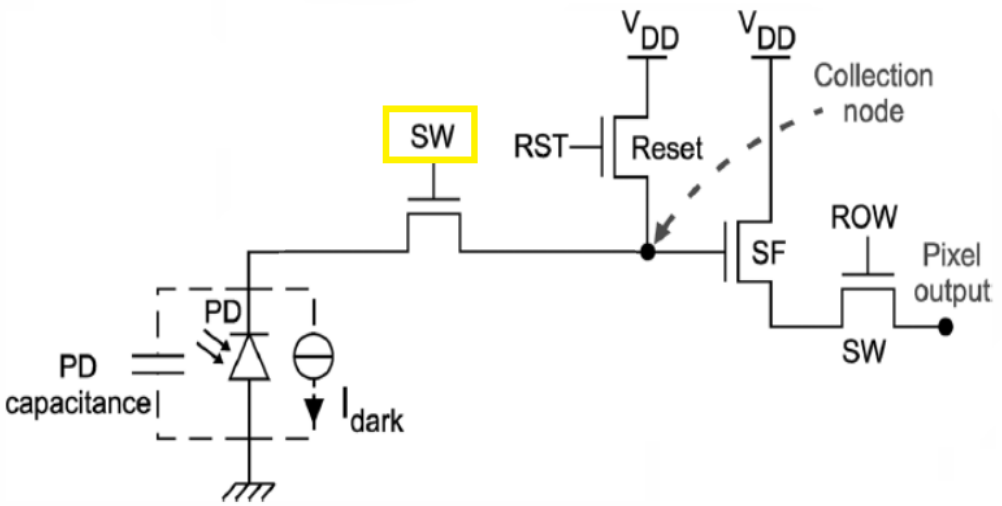
3T Pixel Topology

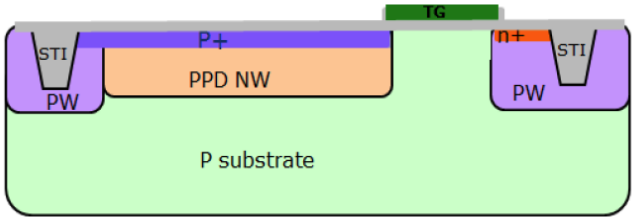


1: reset before integration
2: source follower
3: select
PD: photo diode

- 3 transistors used
- PD exhibits a capacitance due to the space charge region (SCR) of the reverse PN junction
- Dark current discharges the capacitance of the collection node

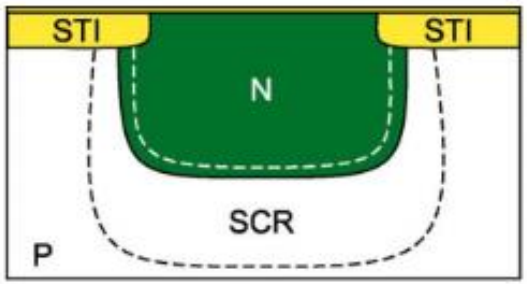
4T Pixel Topology



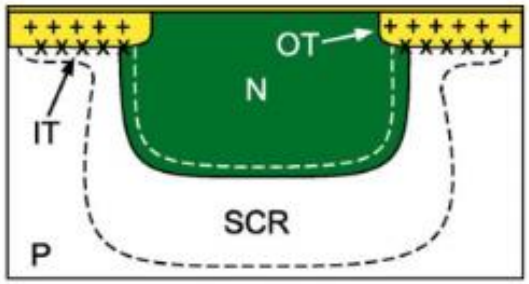


- 1 Megapixel sensor uses 4T pixel topology, Pinned Photodiode (PPD) light-sensitive element
- The pinned photodiode structure uses a shallow p+ layer on top of an n-well layer of a traditional pn junction photodiode. The n well is “sandwiched” between the p+ layer on top and the p epi layer underneath
- A transfer gate is shown as an additional switch (SW), and the collection node is an n+ in p-well floating diffusion
- The PPD is ideal for low light or high-speed applications, such as this DOE program
- Advantages of the PPD and 4T pixel include inherent noiseless gain from PD to the floating diffusion, fast integration and readout times, reduced dark current, lower noise, and increased quantum efficiency

TID-induced Dark Current Increase



(a)



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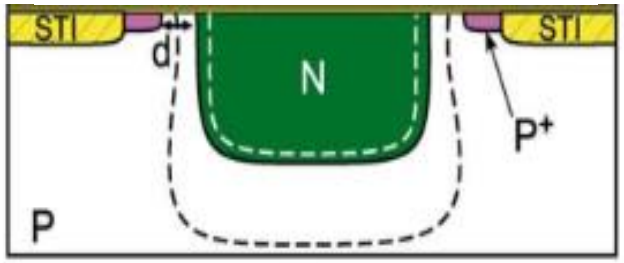
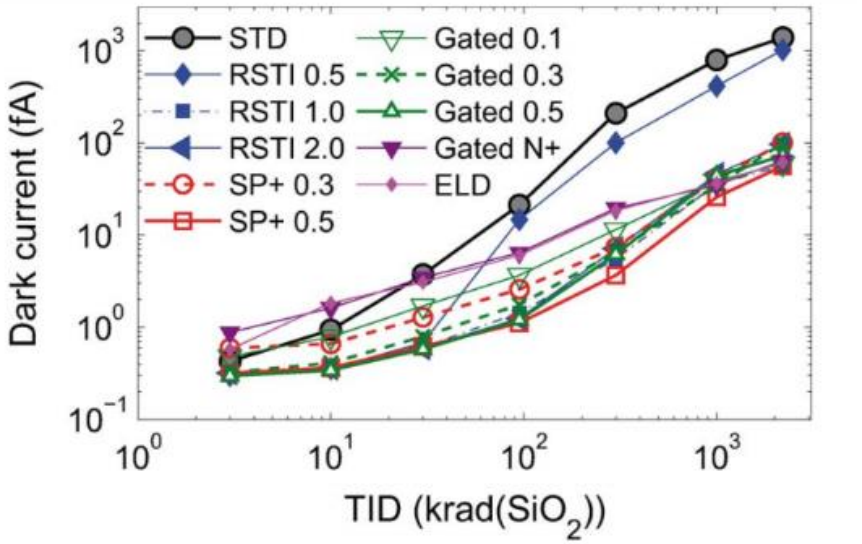


(c)

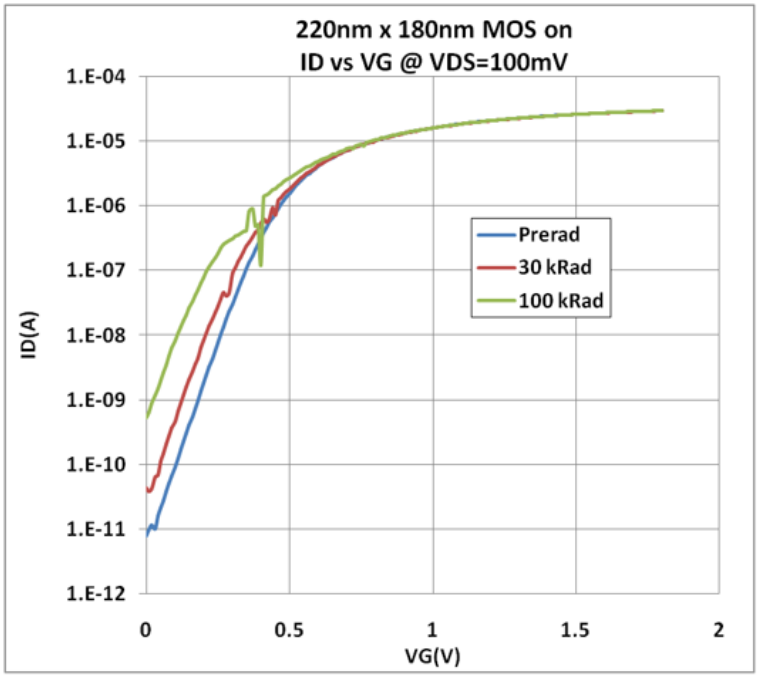
The dark current increase is due to interface trap (IT) and oxide trapped charge (OT) formation along the PD/STI perimeter. Different PD layouts can be used to keep the SCR away from the STI.



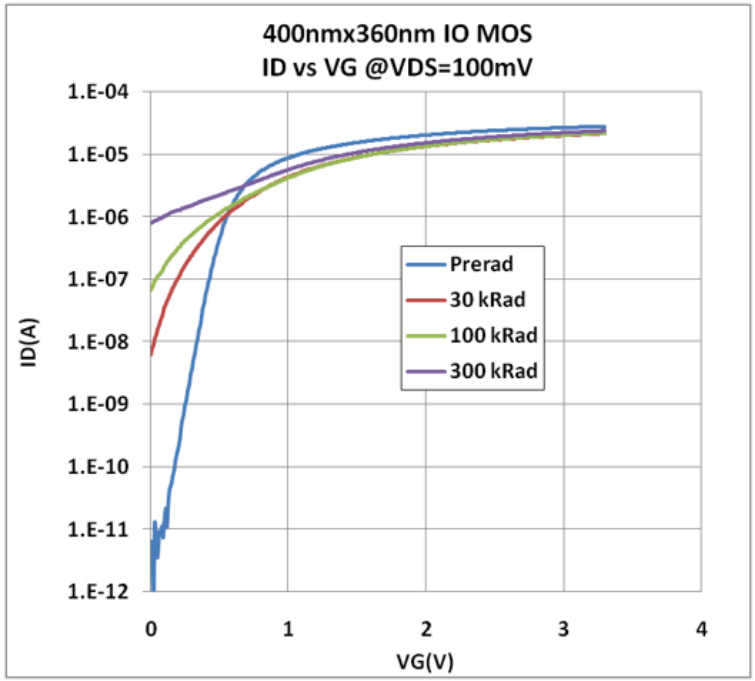
V. Goiffon et al, Generic radiation hardened photodiode layouts for deep submicron CMOS image sensor processes, IEEE TNS vol. 58, n 6, Dec. 2011

180nm CMOS 1.8V vs. 3.3V NMOS Leakage Due to TID

Min. size 1.8V core NMOS



Min. size 3.3V NMOS in the process

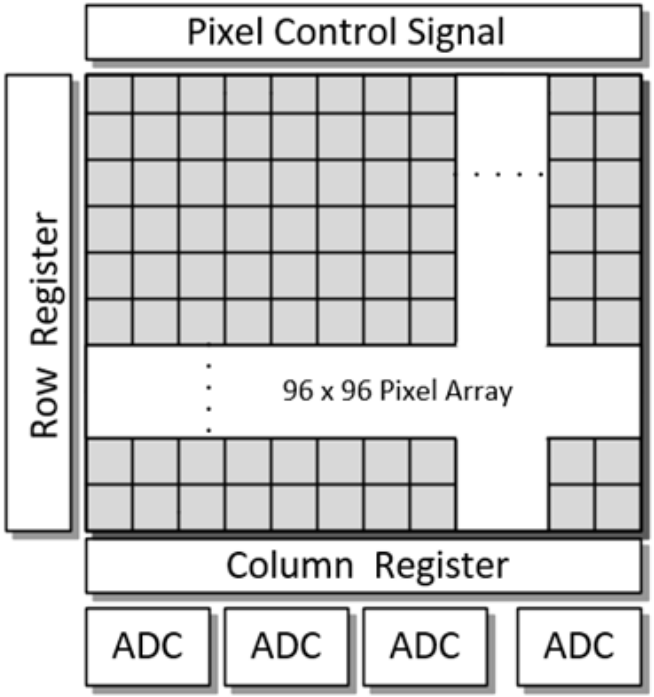


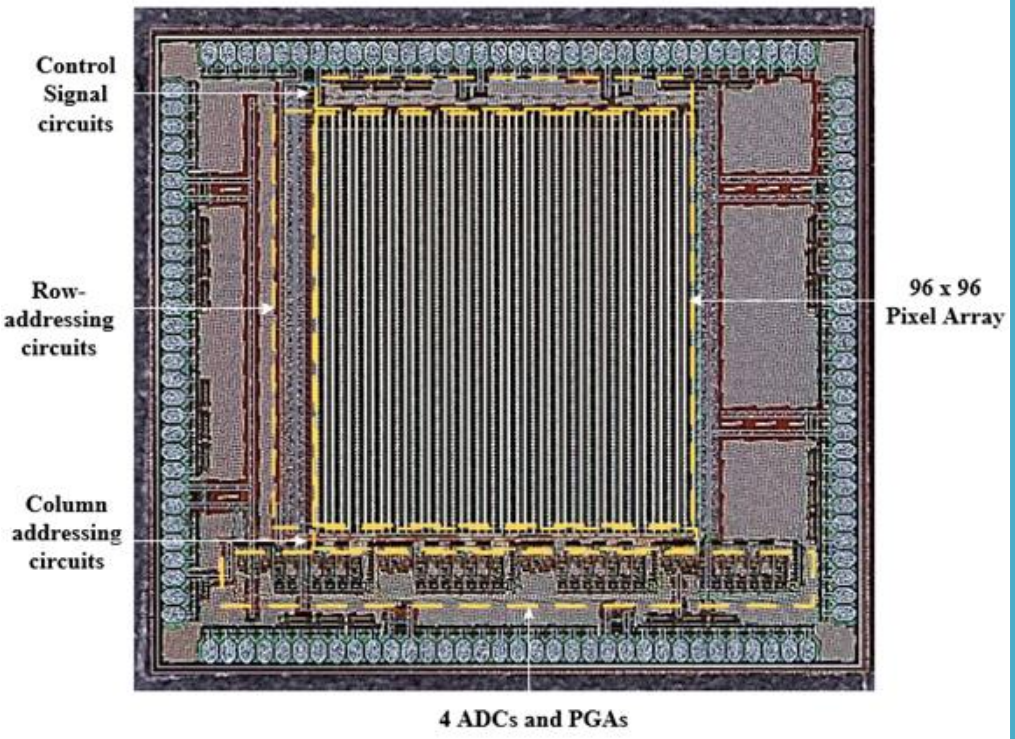
Based on Co-60 tests, the thick oxide NMOS has 100X higher leakage than the core NMOS => Design with 1.8V core transistors

Phase I Summary

- Alphacore completed a tapeout of a 10 kilopixel high-speed CMOS image sensor prototype in Phase I
- The design included the pixel array, programmable gain amplifiers, and ADCs
- The 10 kilopixel sensor was used to build a full prototype camera in the first part of Phase II

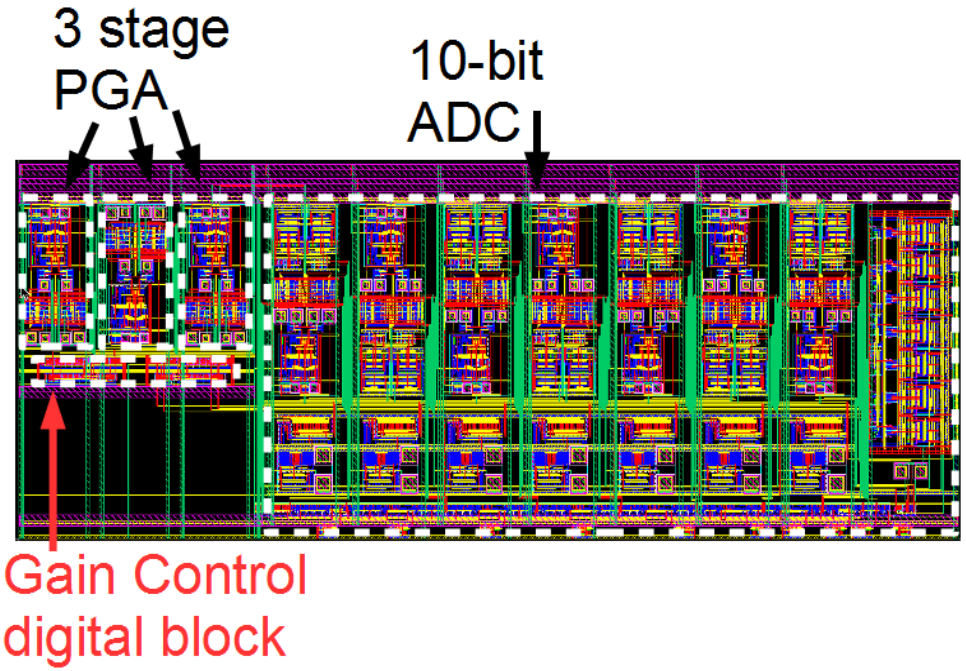
The 10kpix, 10kfps image sensor





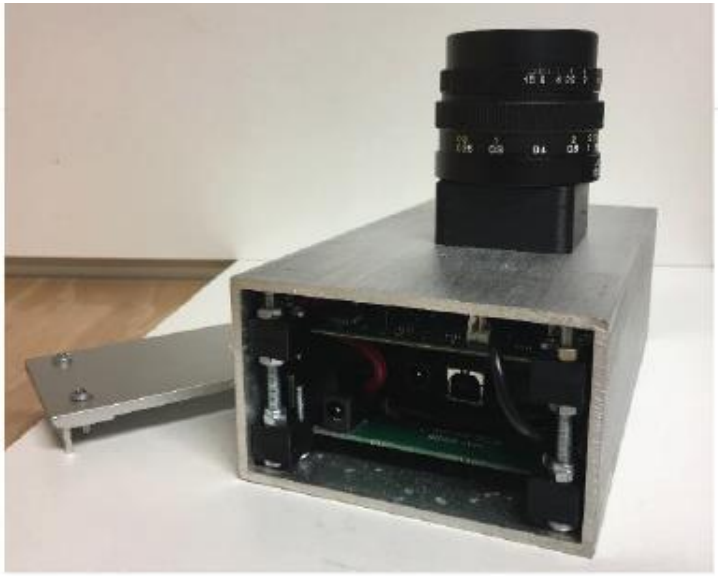
Custom-designed PGA and ADC

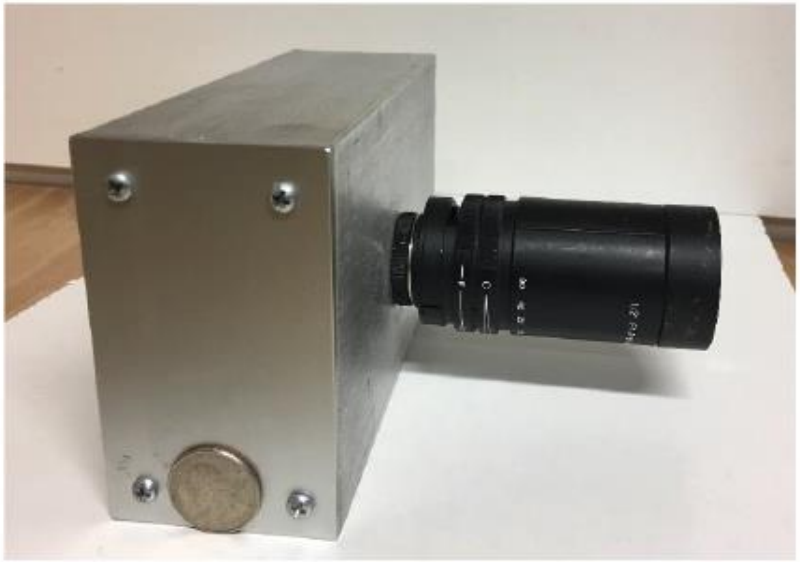
Layout of Alphacore's 10-bit, 50MSPS ADC with Programmable Gain Amplifier



The PGA + ADC consumes 6.4mW. The ADC uses only thin-oxide CMOS 180nm core transistors and does not have BGR, PLL or on-chip configuration or calibration coefficient storage structures.

Prototype Camera Enclosure and Optics





Sample Images

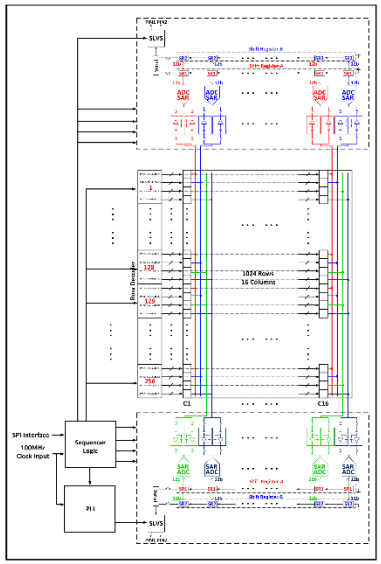
Image taken at 10kfps
(ADCs sampling at 25MSPS)

Image taken at 20kfps
(ADCs sampling at 50MSPS)

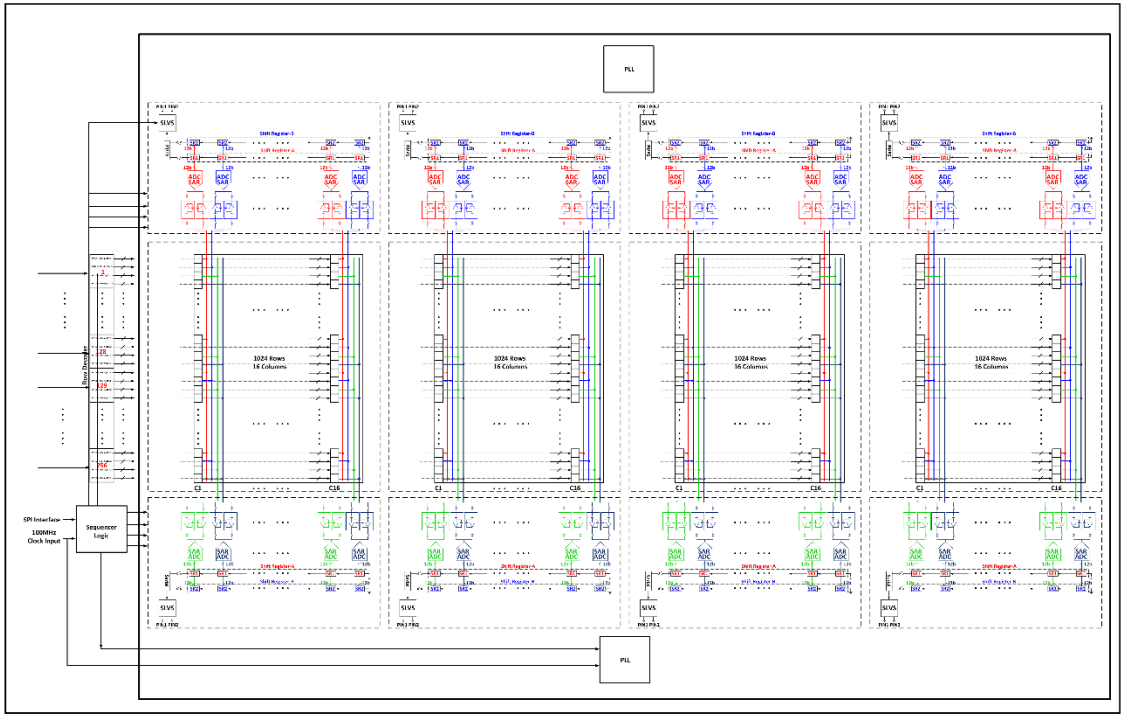
Phase II

- Full 1 Megapixel, 10 kfps chip under development
- Radiation-tolerant design using thin-oxide 1.8V devices for all analog and digital supporting circuits
- Radiation-tolerant pixel design using central T-gate to reduce STI and annular NMOS devices for pixel transistors
- 4 ADCs per column with pipelined data flow (4096 ADCs / chip)
- 12-bit SAR column ADC with 10 µm layout pitch
- Complete solution with on-chip row decoder, digital serial peripheral interface (SPI), control pulse generation, PLL, PGA's, ADC's, biasing, high-speed serializer, low-power scalable low voltage signaling (SLVS) interface
- Radiation tolerant supporting sensor electronics for full radiation tolerant camera solution

Modular 1 Megapixel Sensor Architecture



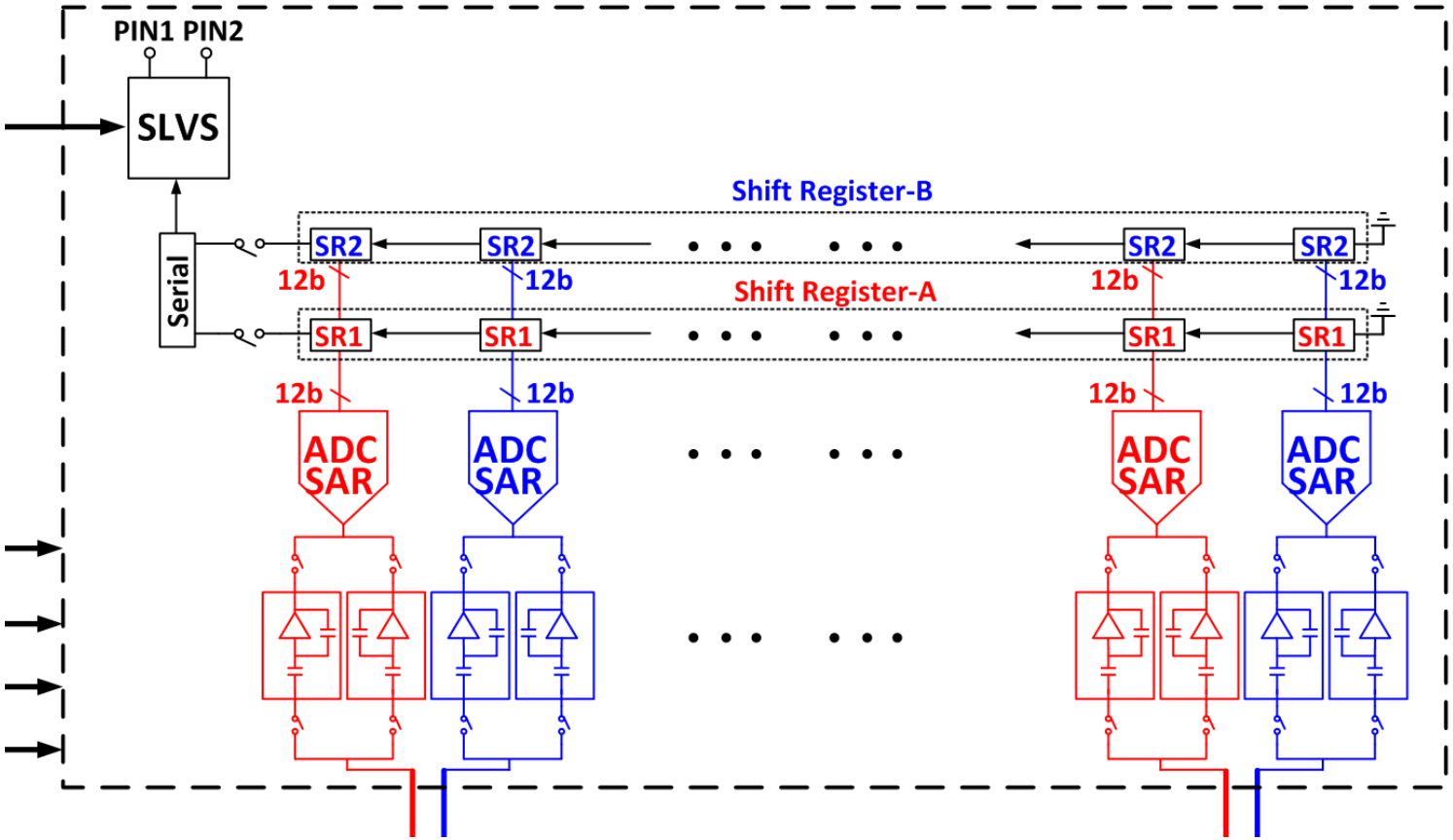
“sub-slice”



“full-slice”

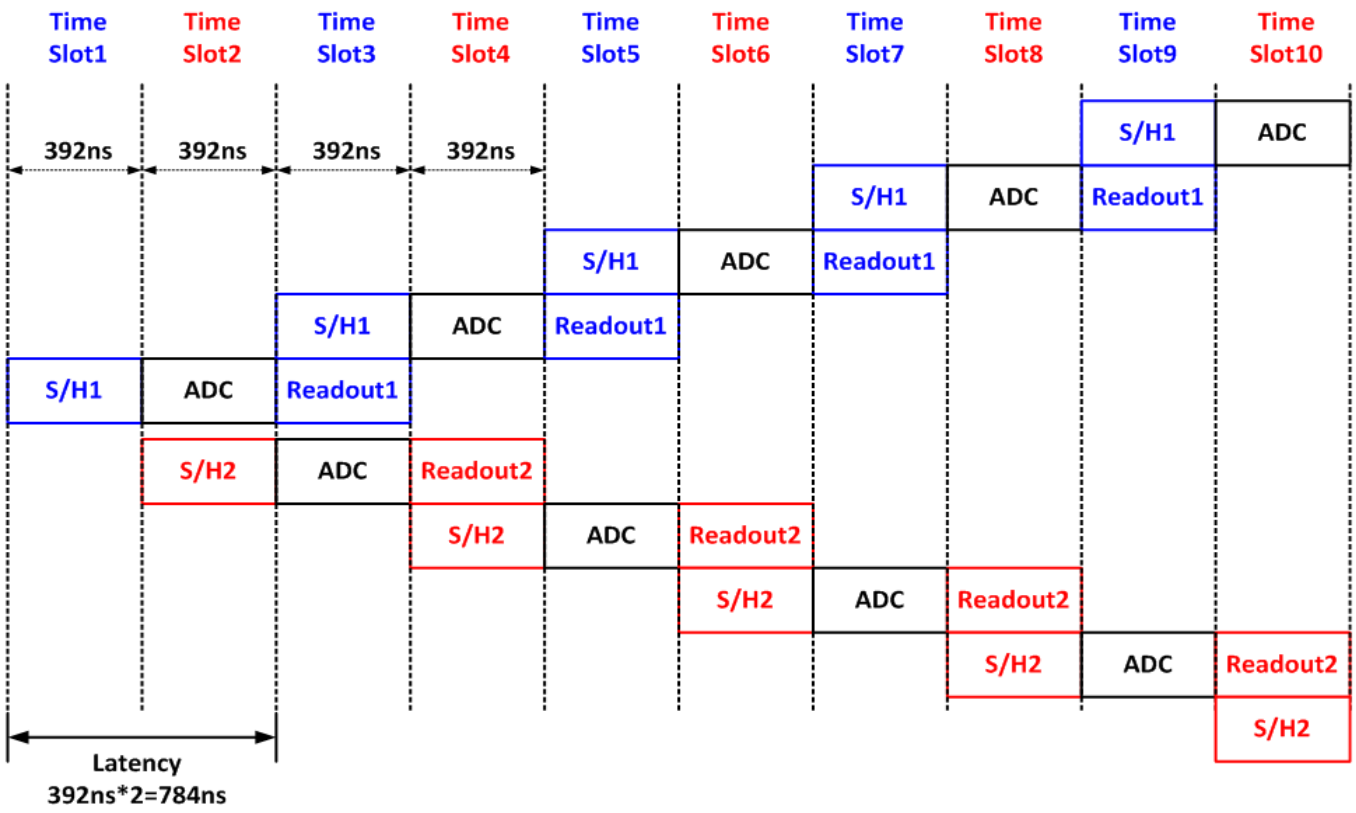
Structure	Summary	Details
Sub-slice	Basic unit	1024 px rows X 16 px columns + 2 SLVS ports
Full-slice	4 sub-slices	1024 px rows X 64 (4x16) px columns + 8 (4x2) SLVS ports
1 Mpx chip	16 full-slices	1024 px rows X 1024 (16x4x16) px columns + 128 (16x4x2) SLVS ports

Pipelined PGA, ADC, Readout



- 2 PGA sample and holds per ADC, plus 4 ADCs per column (two top, two bottom)
- Allows pipelined sampling, conversion, and readout.

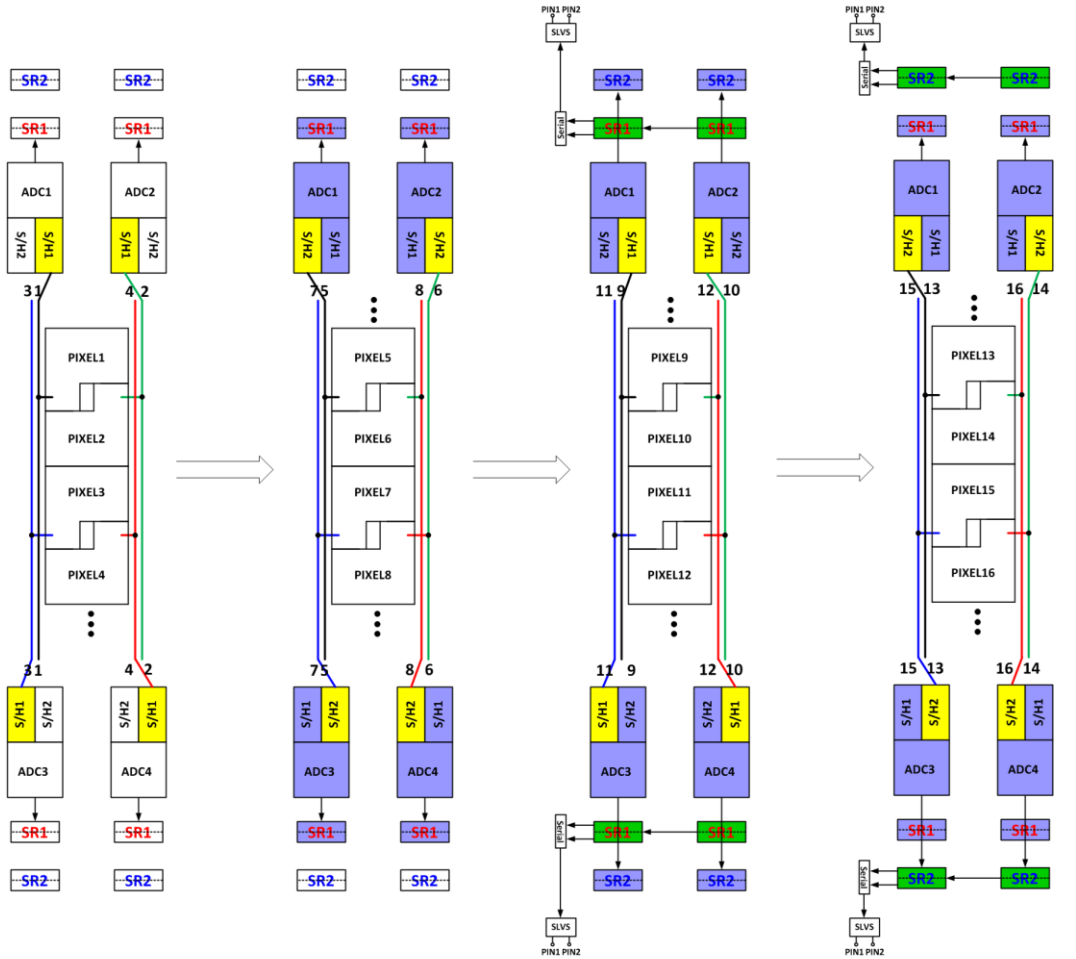
Column Readout Pipelining



The column readout process has 784ns latency before getting digital bits out.
Then each time slot has three operations: one sample and hold, one adc process, and one readout process

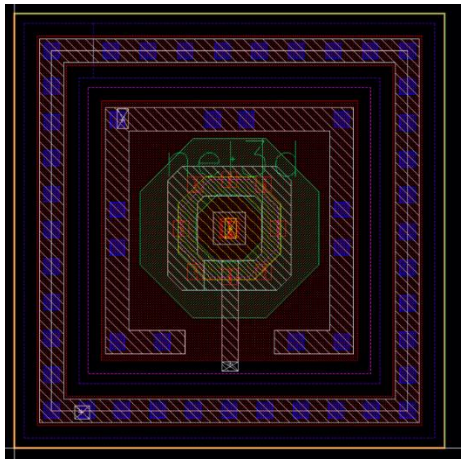
Readout uses novel serializer approach where parallel ADC data is latched to a shift register and thereby ready for high-speed serial transfer at the end of a conversion

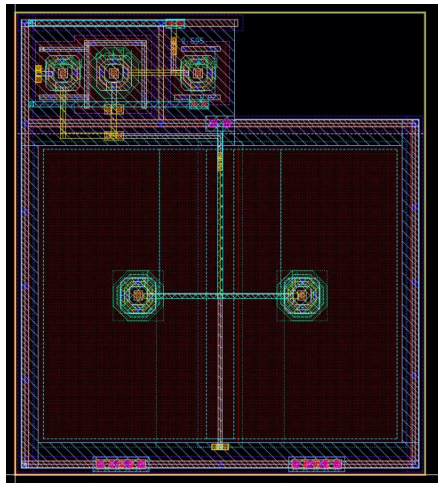
Column Readout Architecture

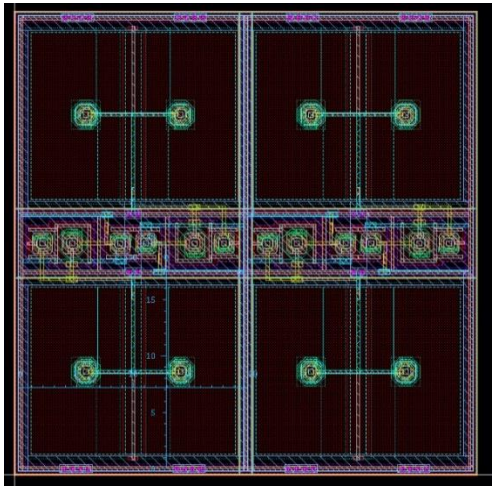


- High-speed 1 Gbps readout architecture
- Pixel values sampled onto PGA
- A to D conversion starts while next pixels are sampled
- Parallel A to D result is shifted out at 1Gbps DDR
- 500 MHz clock generated with on-chip PLL
- SLVS interface has 200 Ohm effective termination and 400 mV supply vs. 50 Ohms and 1.8 V for LVDS → large power savings

Radiation-Tolerant Pixel



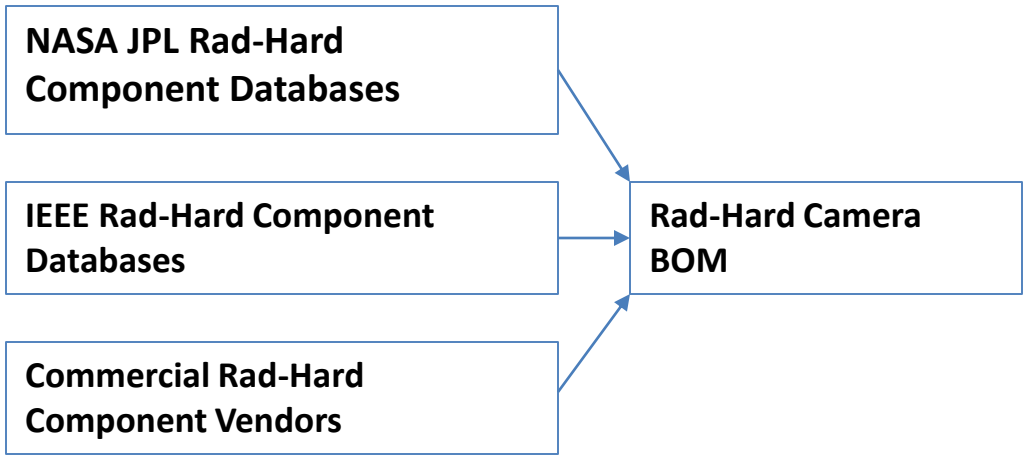




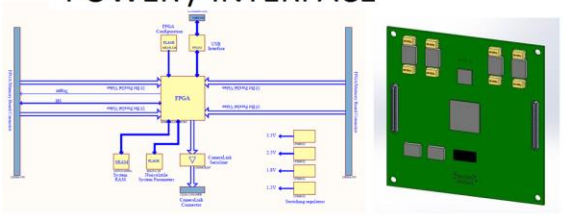
- Annular NMOS devices used for pixel transistors
- Pinned Photodiodes (PPD) offer inherent conversion gain (40µV/e-) ideal for low light, high speed application
- 20µm by 20µm pixel
- Annular transfer gate on the PPD reduces STI and increases radiation tolerance
- Fill factor of 60-65%
- Very fast transfer time of 170 ns or better

Radiation-Tolerant Camera Electronics

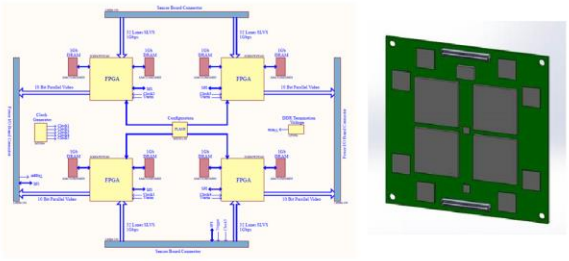
- Camera electronics are modular with pluggable boards for sensor, FPGA, and power/interface
- Interface boards to support multiple protocols (e.g., Camera Link, USB3, GigE Vision)
- Leveraging databases and commercial vendors to create a rad-hard component BOM
- System architecture uses 4 FPGAs and 8 memories to achieve 10 kfps in burst mode



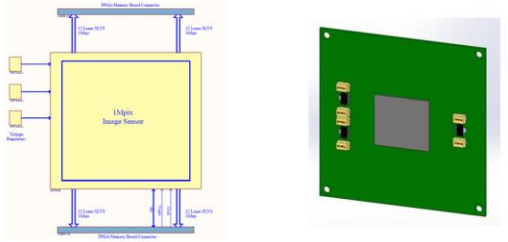
POWER / INTERFACE



FPGA / MEMORY



SENSOR



Future Plans

- Tapeout 1 Megapixel sensor by Sept. 17
- Radiation-hardened camera boards
  - Identify tested components
  - Use qualified components where possible
- Camera-Link frame grabber and GUI
- TID tests for the image sensor
- Upgrade the camera to be compatible with space applications
  - Single event effects and displacement damage need to be considered
  - Size, weight, and power (SWaP) optimization

Summary

- Status after SBIR Phase I and 15 months of Phase II development program for a radiation-tolerant high-speed image sensor and camera has been presented.
- First prototype of a radiation-hard high-speed camera has been constructed and tested.
- Funded application is for particle beam monitoring and diagnostics; other rad-hard/high-speed applications are sought.
- The system is a modular 10kilopixel, 10kfps complete camera with a custom-designed image sensor.
- The architecture is modular and the work to extend it to 1 Megapixel is underway.
- Work to harden the camera board is underway as well.
- Radiation testing of the 1 Mpixel camera expected in early 2018.
- We are considering requirements for space environments.

Questions? Thank you!

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