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Instruments that advance the art

High Density Low Cost Readout Electronics for Large Scale Radiation Detectors

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DOE Office of Science, Office of Nuclear Physics

Presenter: Dr. Stephen Asztalos, XIA LLC

Motivation

- **Large scale nuclear physics experiments with hundreds or thousands of detector channels**
  - Existing off-the-shelf readout electronics prohibitively expensive
  - Need for high density, low cost readout electronics with good linearity, timing and energy resolutions

- **Recent improvements in the design of commercial ADCs have resulted in a variety of multi-channel ADCs that are natural choice for designing such high density readout modules**
  - 4 or 8 channels integrated on a single chip
  - 10 to 16 bits and 40 to 250 MSPS sampling rates
  - Consume power as low as ~50 mW per channel

Large Scale NP Detectors

- **Boo**ster **N**eutrino **E**xperiment (BooNE) at Fermilab
  - Investigate the question of neutrino mass by searching for oscillations of muon neutrinos into electron neutrinos
  - MiniBooNE, the first phase of BooNE, uses a single detector which is a large tank of 800-ton mineral oil liquid scintillator and viewed by 1280 photomultiplier tubes >1280 readout channels needed
- **A**bsolute **L**uminosity **F**or **A**TLAS (ALFA)
  - Each detector module consists of ten layers of two times 64 scintillating fibers each
  - The fibers are coupled to 64-channel Multi-Anodes PMTs
  - The total number of channels is about 15000
- GRETINA, the first stage of a full **G**amma-**R**ay **E**nergy **T**racking **A**rray (GRETA)
  - A large number of auxiliary detectors are planned for GRETINA, e.g. silicon and scintillation particle detectors and gas counters

SBIR Project Objectives

SBIR Project objective is to develop a high channel count, low cost, and versatile digital readout module for large scale nuclear physics radiation detectors

- "Pixie-32": a 32-channel digital gamma-ray spectrometer
- target price per channel will be only $200-$300 while it will still be a true spectrometer
- Implement a PCI Express interface (up to 1 GB/s) on Pixie-32 modules (versus the regular 100 MB/s PCI interface on Pixie-4 and Pixie-16)

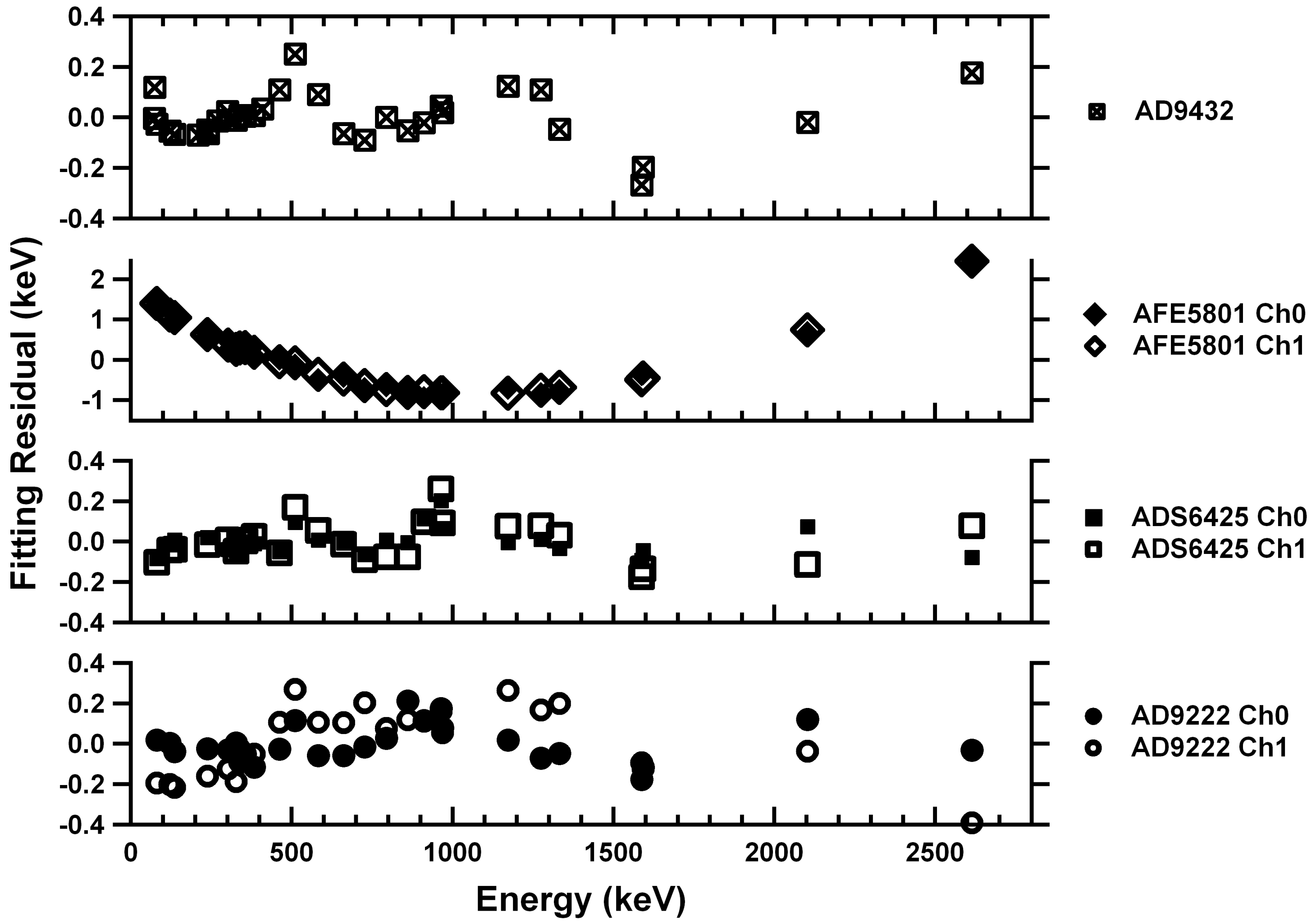
Technical Approach

SBIR Phase	Tasks	Status
I	Verify capability of modern FPGAs to receive Gbit/s data streams from a multichannel ADC	Done
I	Estimate costs for different board architectures	Done
I	Verify multichannel ADCs for spectroscopy quality	Done
II	Finalize architecture for the Pixie-32 spectrometer	Done
II	Draw design schematics and layout printed circuit boards	Done
II	Manufacture a small number of prototype boards	Done
II	Develop Pixie-32 FPGA firmware	Done
II	Develop PCI Express driver and API library	90%
II	Develop a user interface that can be used for 100's or even 1000's of data acquisition channels	In Progress

No-cost extension until November 2015

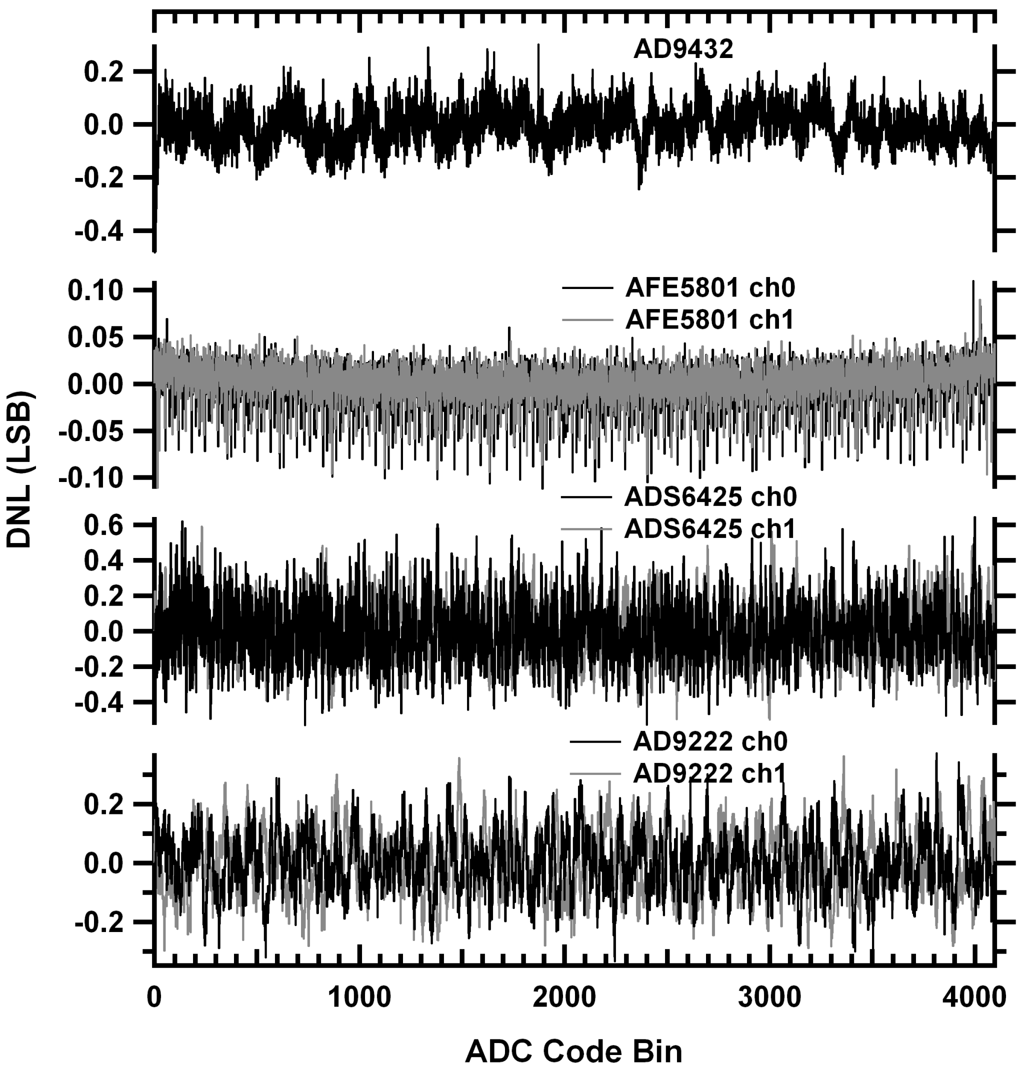
Multichannel ADC Tests

Integral Nonlinearity (INL) Tests of Multichannel ADC



Multichannel ADC Tests

Differential Nonlinearity (DNL) Tests of Multichannel ADC



Chosen Multichannel ADC – AFE5801

8-Channel Variable-Gain Amplifier (VGA) With Octal High-Speed ADC

Eight Variable-Gain Amplifiers (VGA)

Variable Gain, –5dB to 31dB With 0.125dB or 1dB Steps

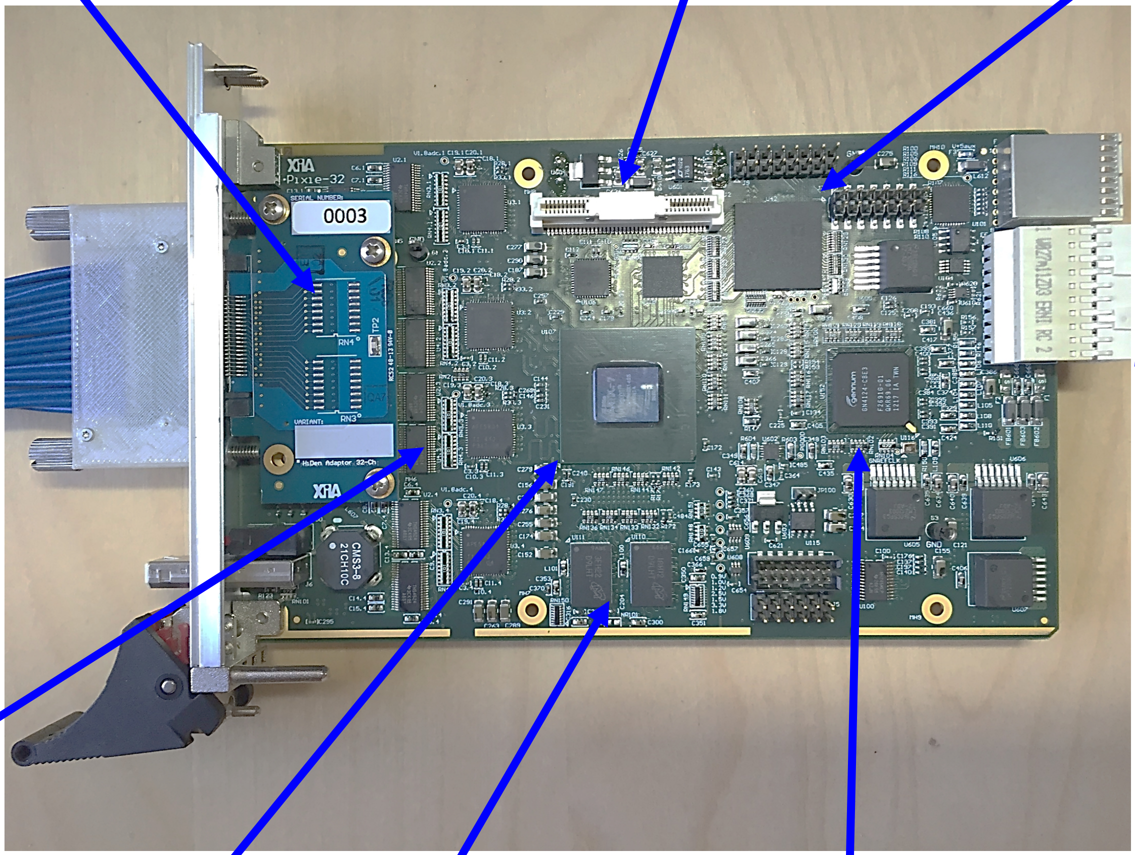
Digital Gain Control

Third-Order Antialiasing Filter With Programmable Cutoff Frequency (7.5, 10, or 14MHz)

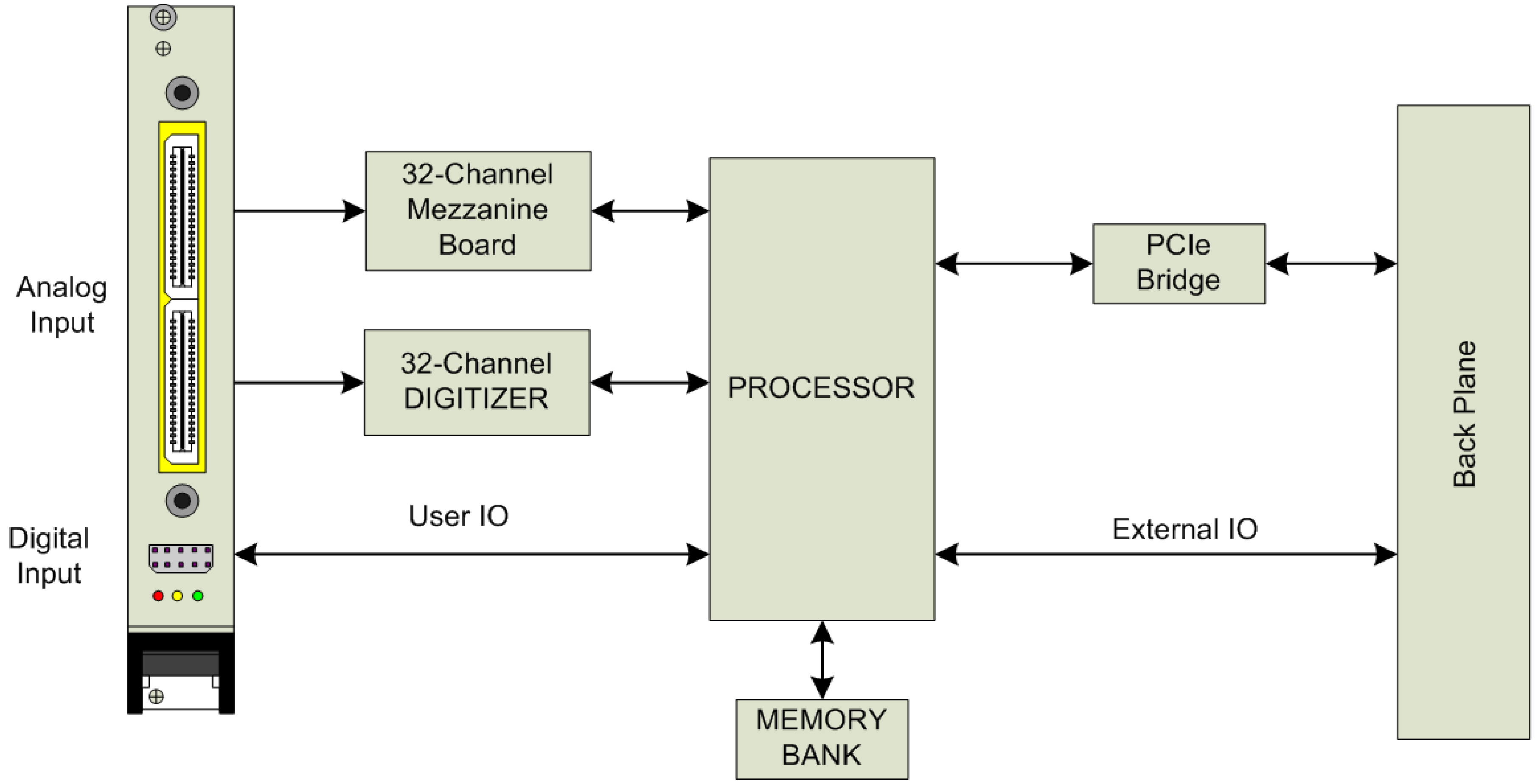
Analog-to-Digital Converter (ADC)

Octal Channel, 12Bit, 65MSPS

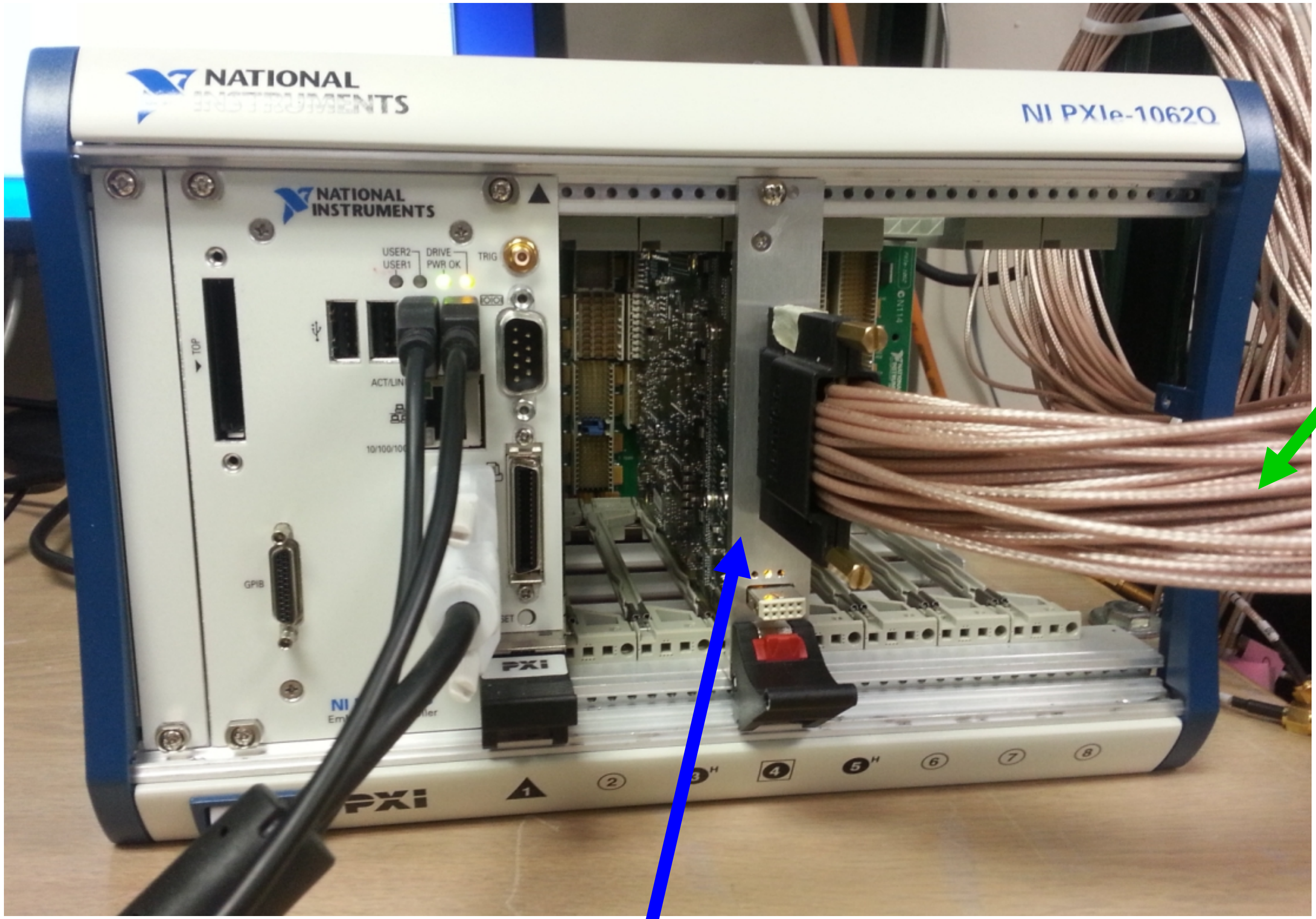
Pixie-32 Prototype



Pixie-32 System Diagram



Pixie-32 Prototype



Pixie-32 in a PXIe chassis

32 single-ended analog signal inputs to the Pixie-32 front panel

Other types of cabling solutions are possible, e.g. ribbon cable connections to detector outputs

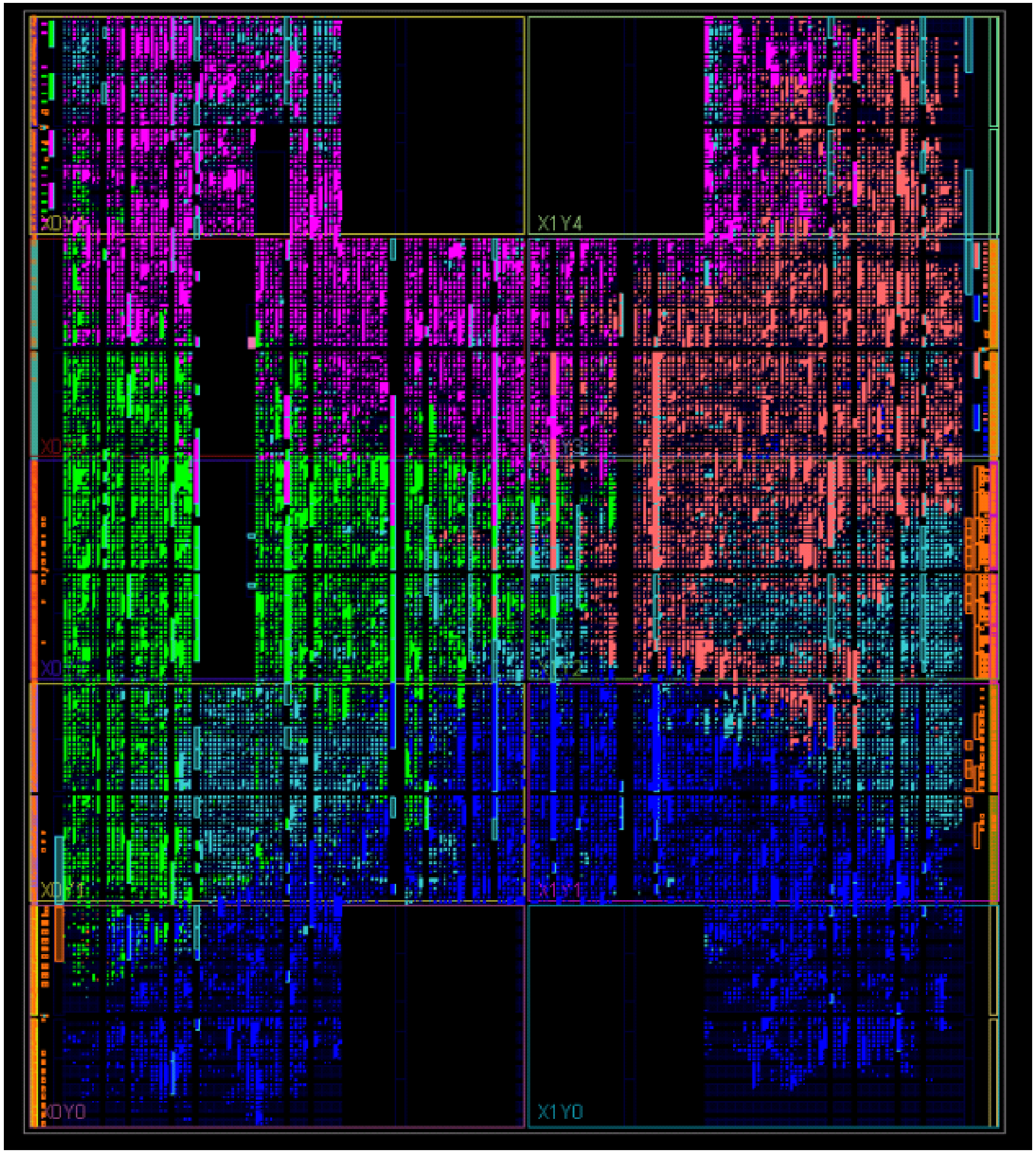
Main Processor FPGA

Instruments That Advance The Art

- Utilized the latest FPGA technology, a 7-series Artix-7 FPGA from Xilinx, which offers low power, low cost and yet high performance, when compared to existing FPGA technology
- Firmware runs inside this Artix-7 FPGA
  - deserialize high speed serial data from ADCs
  - trigger and compute detected pulses' energy, time of arrival, and record raw waveforms for offline pulse shape analysis
  - communicate to host computer through a up to 800 MB/s PCI-express interface

32-Chan Logic in Artix-7 FPGA

- Four 8-chan groups of logic indicated by the four colored regions in the Artix-7 FPGA
- Slices utilization percentage is only 23% for 32 channels

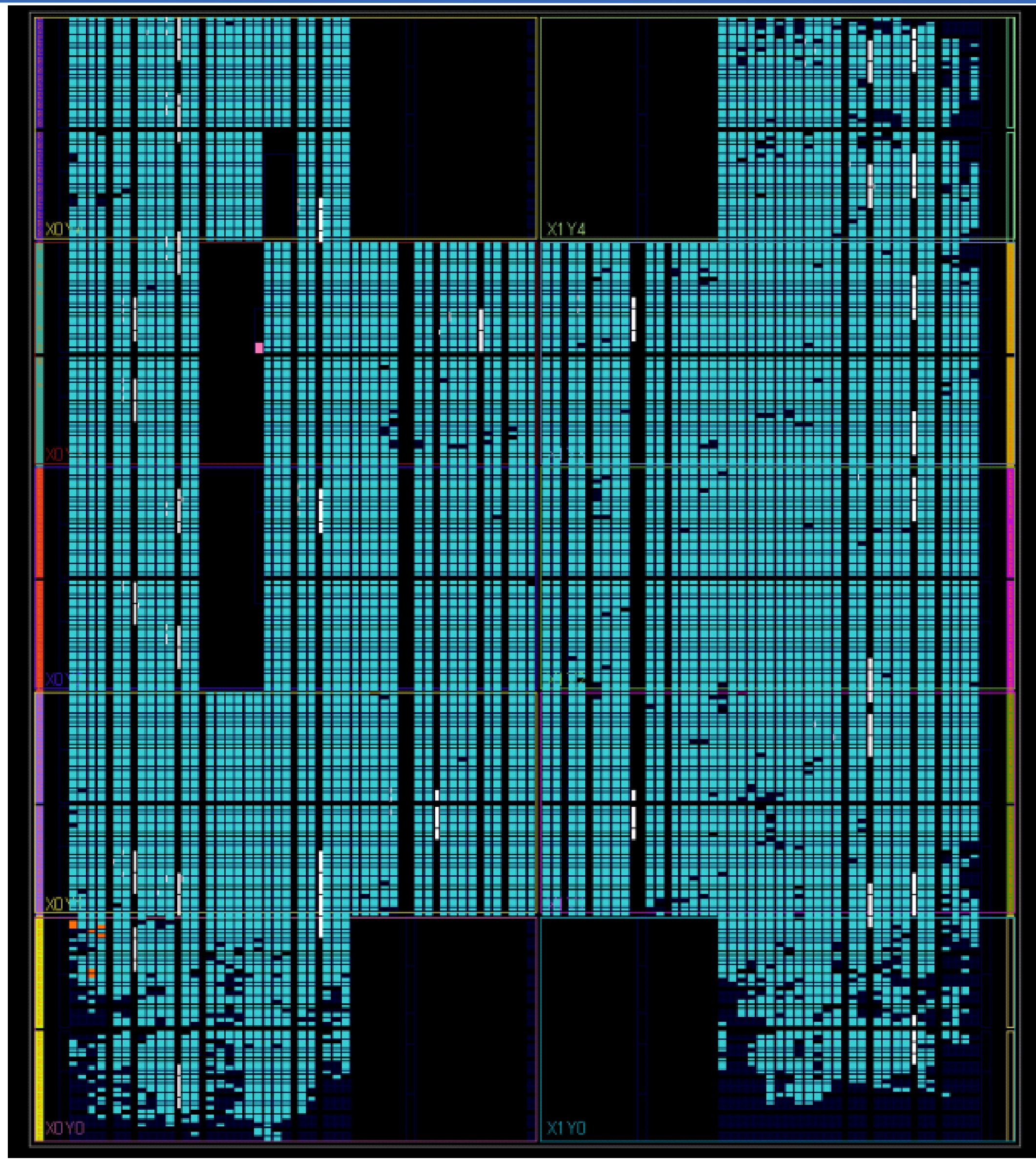


DSP Slices in Artix-7 FPGA

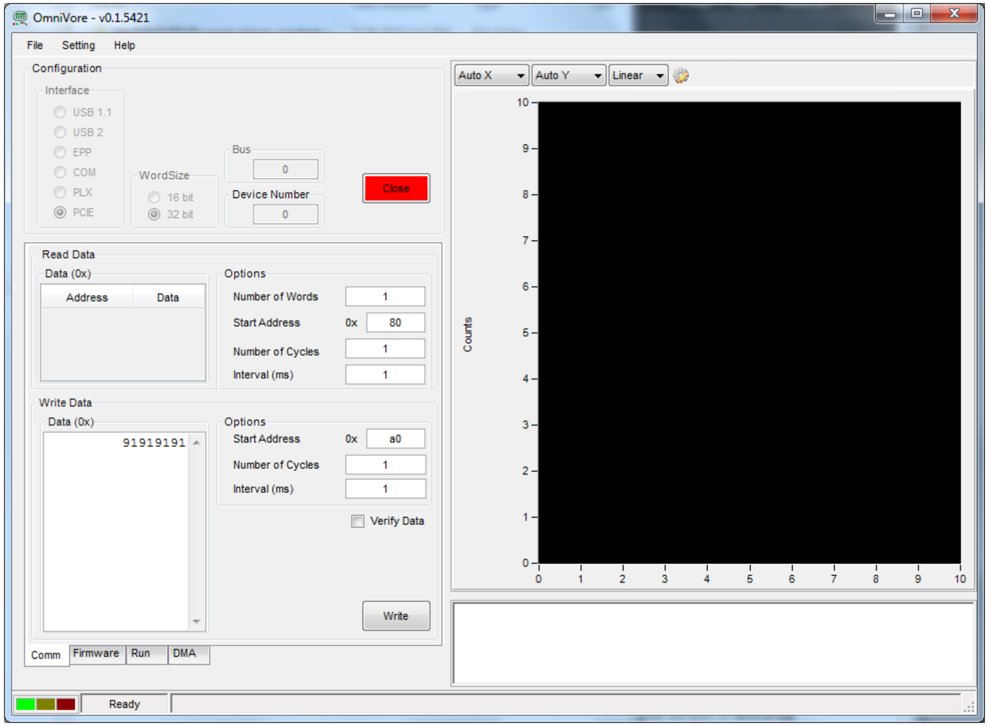
XIA Instruments That Advance The Art

- Utilized DSP slices in Artix-7 FPGA to compute pulse energy

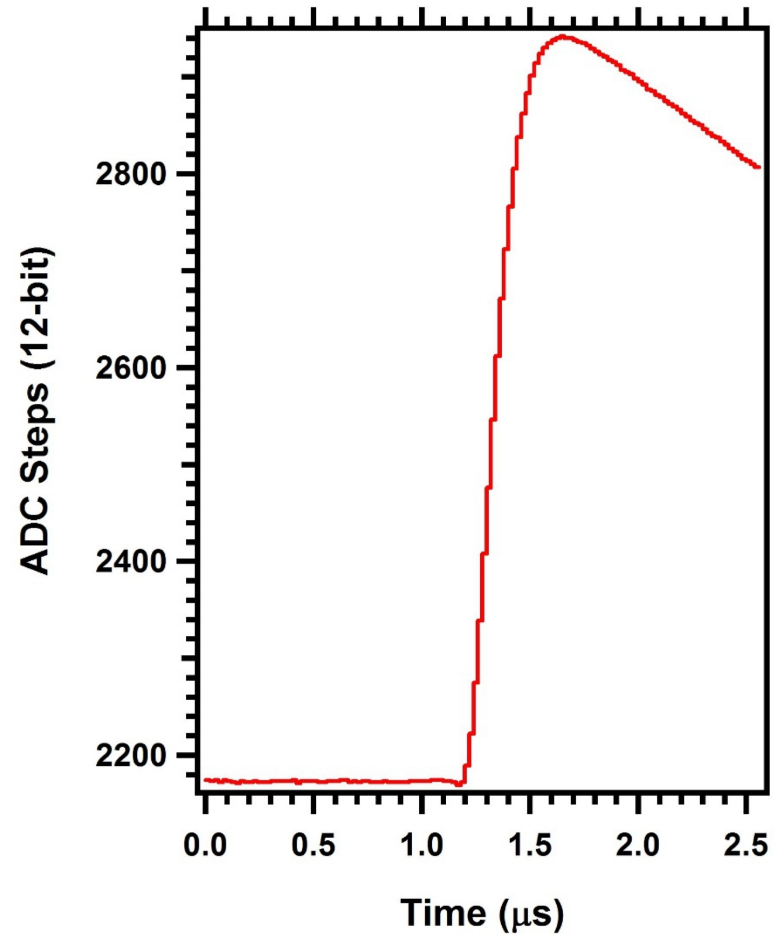
- DSP slices have 25 x 18 multiplier, 48-bit accumulator, and pre-adder



Pixie-32 Test Software



Sample trace captured by Pixie-32



- Software for booting up Pixie-32 boards
- Direct FPGA register read/write
- Data acquisition and display

Phase II Remaining Tasks

- Complete the development of PCI Express driver and API library and the user interface software
- Test & Characterization
  - Characterize gamma-ray spectroscopy performance
  - Test Pixie-32 at collaborating laboratories

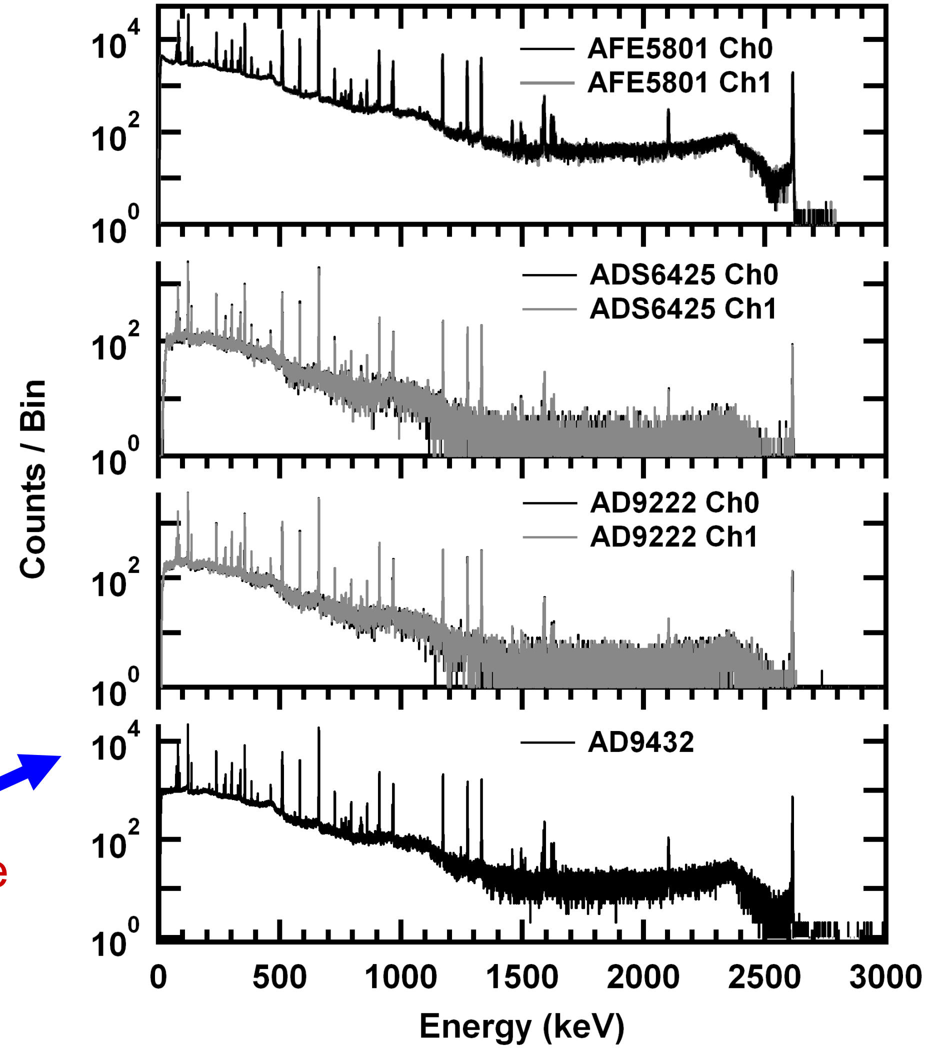
Summary & Outlook

- Characterized spectroscopy performance of multichannel ADCs
- Finalized Pixie-32 board architecture
- Designed and manufactured Pixie-32 prototype boards
- Working to complete the development of firmware and software for the Pixie-32

- Ongoing efforts to commercialize Pixie-32 as early as possible (orders already pending!)

Multichannel ADC Tests

ADC	#Chan	Rate (MSPS)	Bits
AD9222	8	65	12
ADS6425	4	125	12
AFE5801	8	65	12
AD9432	1	100	12



Energy spectra from a 40% coaxial HPGe Detector and multiple radiation sources

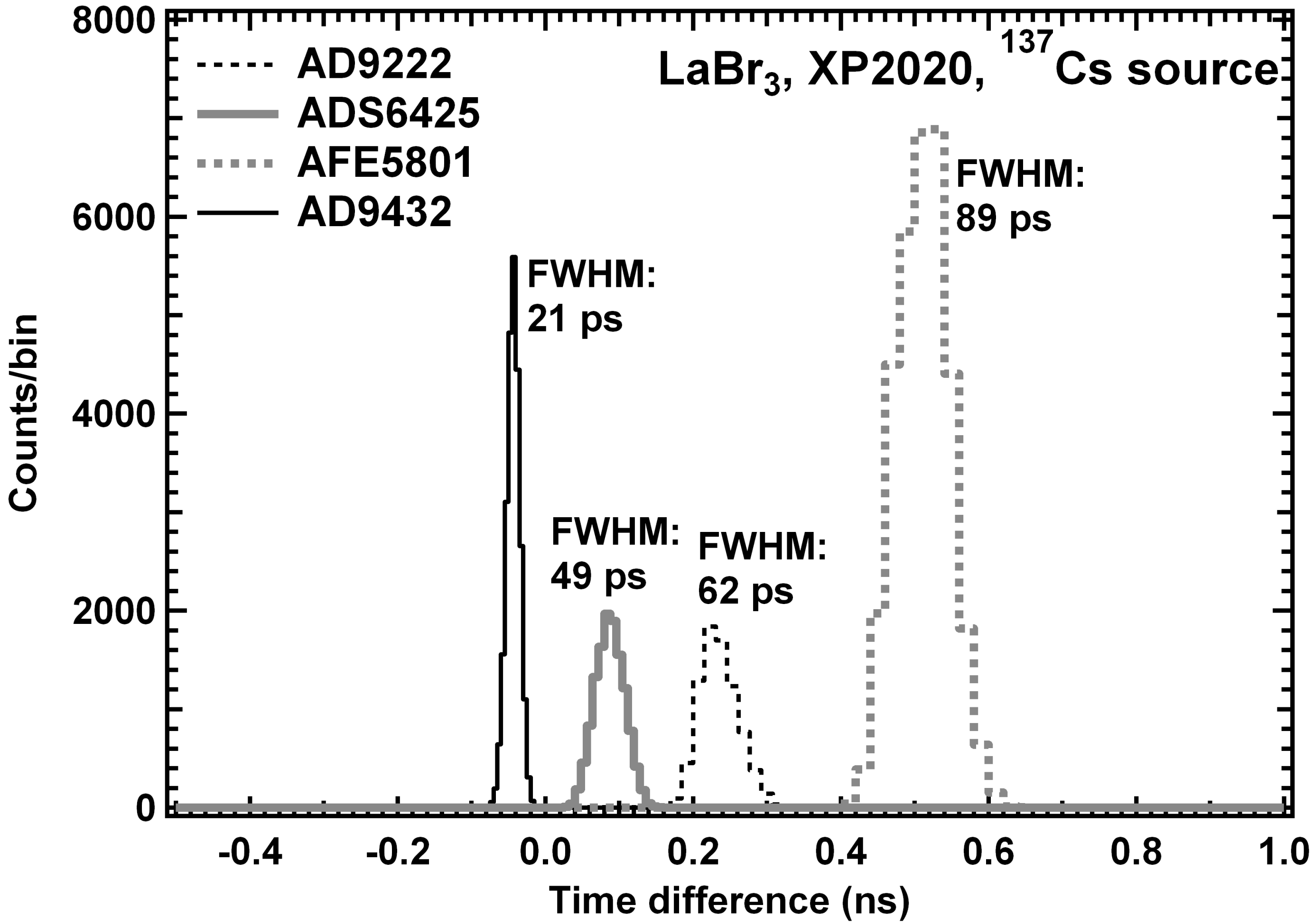
Multichannel ADC Tests

HPGe energy resolution (keV, FWHM)

Energy (keV)	AD9222		ADS6425		AFE5801		AD9432
	Ch0	Ch1	Ch0	Ch1	Ch0	Ch1	
122	0.92	0.92	0.98	1.08	1.15	1.16	0.84
661.6	1.34	1.36	1.36	1.43	1.55	1.55	1.28
1332.5	1.78	1.80	1.84	1.82	1.96	1.96	1.72
2614.5	2.39	2.44	2.47	2.52	2.64	2.63	2.36

Multichannel ADC Tests

Timing resolution measured using a single $LaBr_3$/PMT detector and a ^{137}Cs source. The output of the $LaBr_3$/PMT was split into two branches and then fed into two ADC channels.



Pixie-32 Block Diagram