Low Cost, High-Density Digital Electronics for Nuclear Physics

Wojtek Skulski

Principal Investigator

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The company and its capabilities

The main focus of SkuTek is data acquisition (DAQ) instrumentation. Our instruments use digital techniques to acquire and process signals from nuclear radiation detectors.

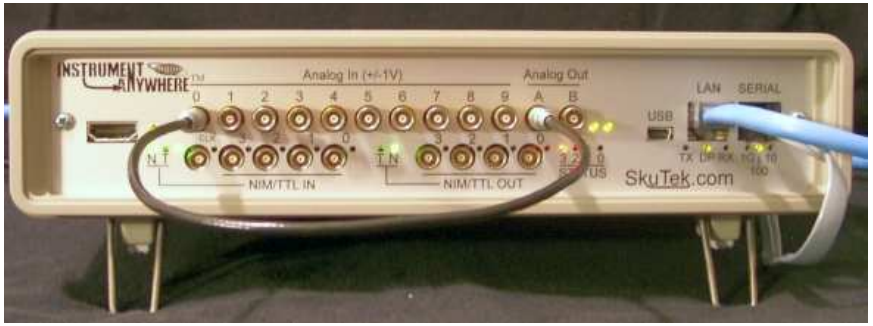
We work in tight collaboration with our key customers, focusing on instrumentation for nuclear physics, high energy physics, and particle astrophysics.

Our capabilities:

- Electronic design “top to bottom”: from the requirements, through schematic capture and board layout, all the way to prototyping, production, and support.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, with special focus on Embedded Linux.
- Graphical User Interfaces for our instruments.
- Algorithms for data processing.

Our capabilities

Standalone networked digitizer



VME digitizer

Description of Phase II project

Problem or situation that is being addressed.

The channel count of modern Nuclear Physics experiments has increased into thousands. There is need for cost effective, high density data acquisition (DAQ) systems with many thousands of channels capable of *in situ* signal analysis.

How this problem or situation is being addressed.

We are developing digital DAQ modules with dozens of channels of waveform digitization, on-board FPGA, Ethernet, USB-2, and VME interfaces, and running Linux on-board. The digitizers participate in a novel system architecture that will enable building DAQ systems with thousands of channels.

Our approach.

We work in a close collaboration with our scientific customers to help them solve their problems in the most effective way.

Relevance to the NP program

The electronics developed through this grant will be extremely scalable, from a single-channel table-top units, all the way to systems with thousands of channels.

The table top units will serve small NP experiments, radiation detector development, or student labs teaching Nuclear Physics.

Larger systems will serve experiments conducted at DOE facilities, e.g., Facility for Rare Isotope Beams (FRIB), which is a new national user facility for Nuclear Physics.

I will show more details after presenting our products.

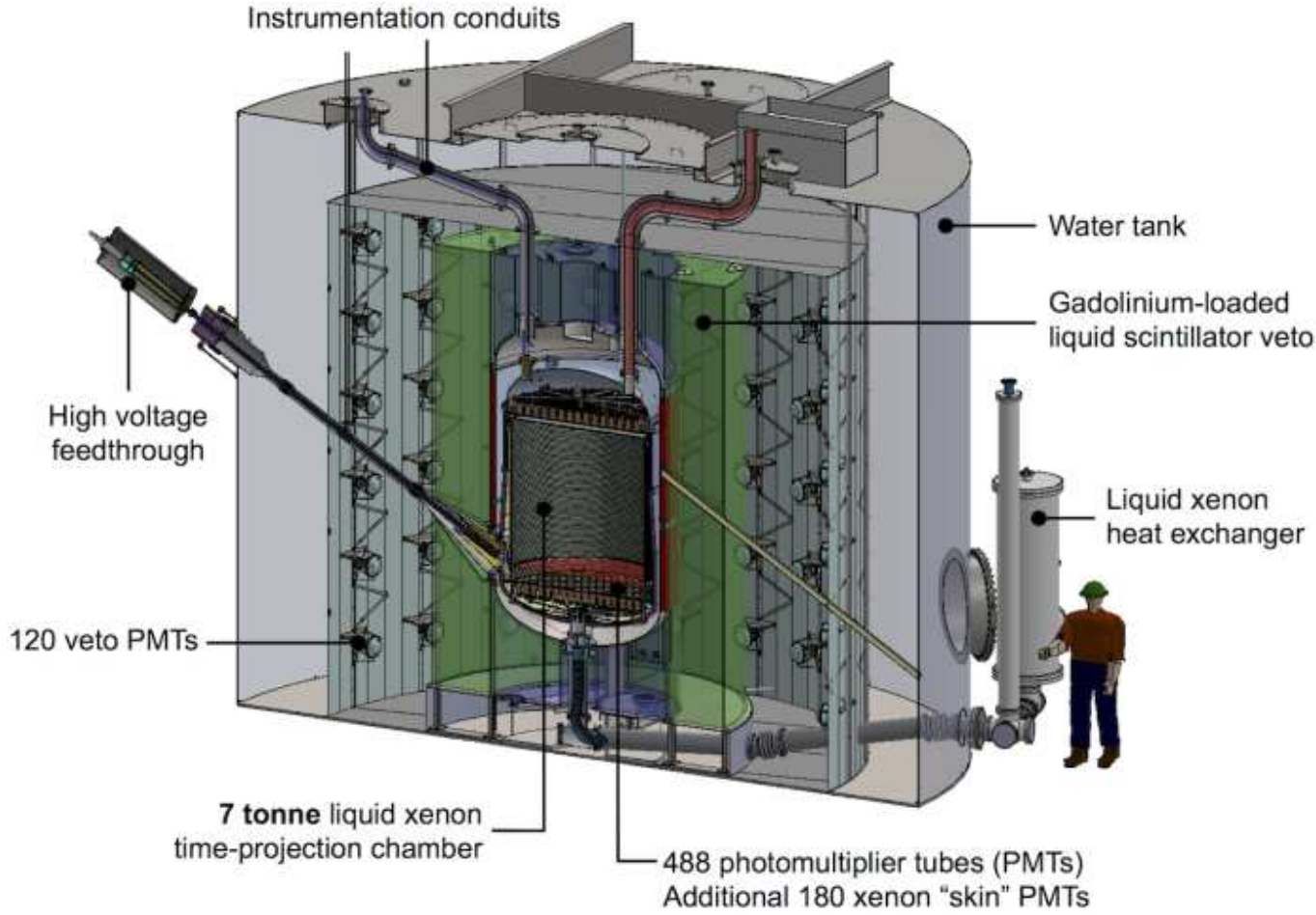
Example detector served by our DAQ electronics

SkuTek collaboration with UofR Physics and Astronomy

LZ is the “ultimate Dark Matter Search Detector” under development by 32 institutions.
We are building the digital DAQ for LZ with 1,276 channels.

- Amount of Xenon:
  - 5.6 tons fiducial
  - 7 tons in the vessel
  - 10 tons total.
  - Drift time in Xenon: 700 μs.
- Number of PMTs:
  - 488 main volume (dual gain)
  - 180 “skin”
  - 120 veto
  - Total **788** PMTs.
- Electronic channels:

  2*488 + 180 + 120 = **1,276**.



DAQ Architecture with Digitizers, Logic Units, and Collectors.

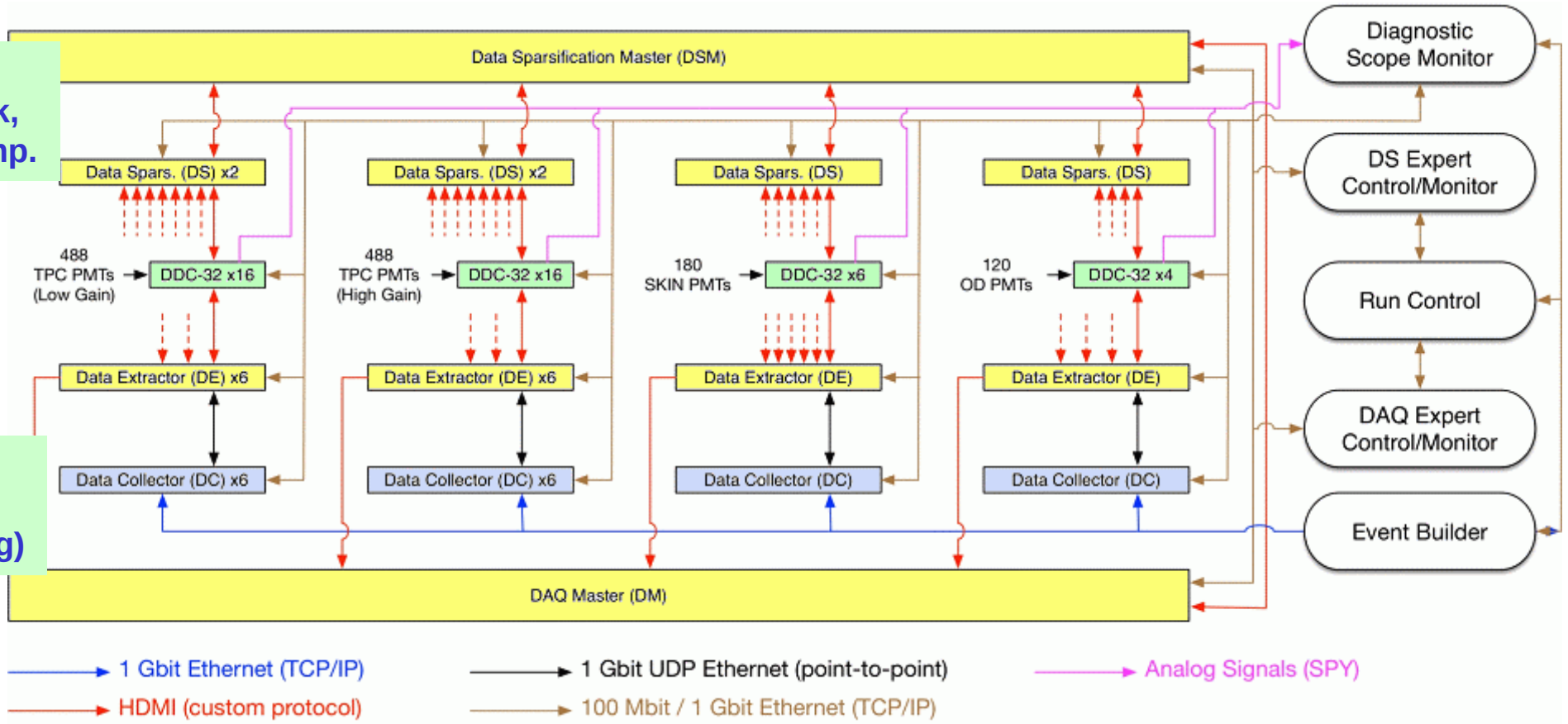
How our developments will be used for LZ

- **42 digitizers**: 32 channels, 14 bits @ 100 MSPS, low noise (~1.3 LSB).
- **22 logic units**: event preprocessing and real time sparsification. Also ADC clock and time stamp.
- **14 data collectors**: off-the-shelf PC units and disk arrays.
- Total data rate that the DAQ can potentially handle: 14 collectors * ~100 MB/s each = 1,400 MB/s.
- Cost effective thanks to high channel density (32 ADC's per digitizer).
- Trigger and the DAQ integrated using fast point-to-point SerDes links.

SkuTek collaboration with UofR Physics and Astronomy

Trigger, ADC clock, Time stamp.

Data Readout (streaming)



Deliverables

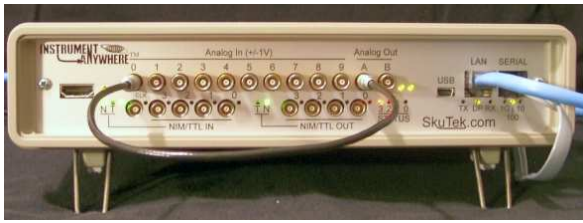
DAQ Modules and DAQ Systems for Nuclear Physics applications.

Some groups need to add individual DAQ modules to their existing systems.

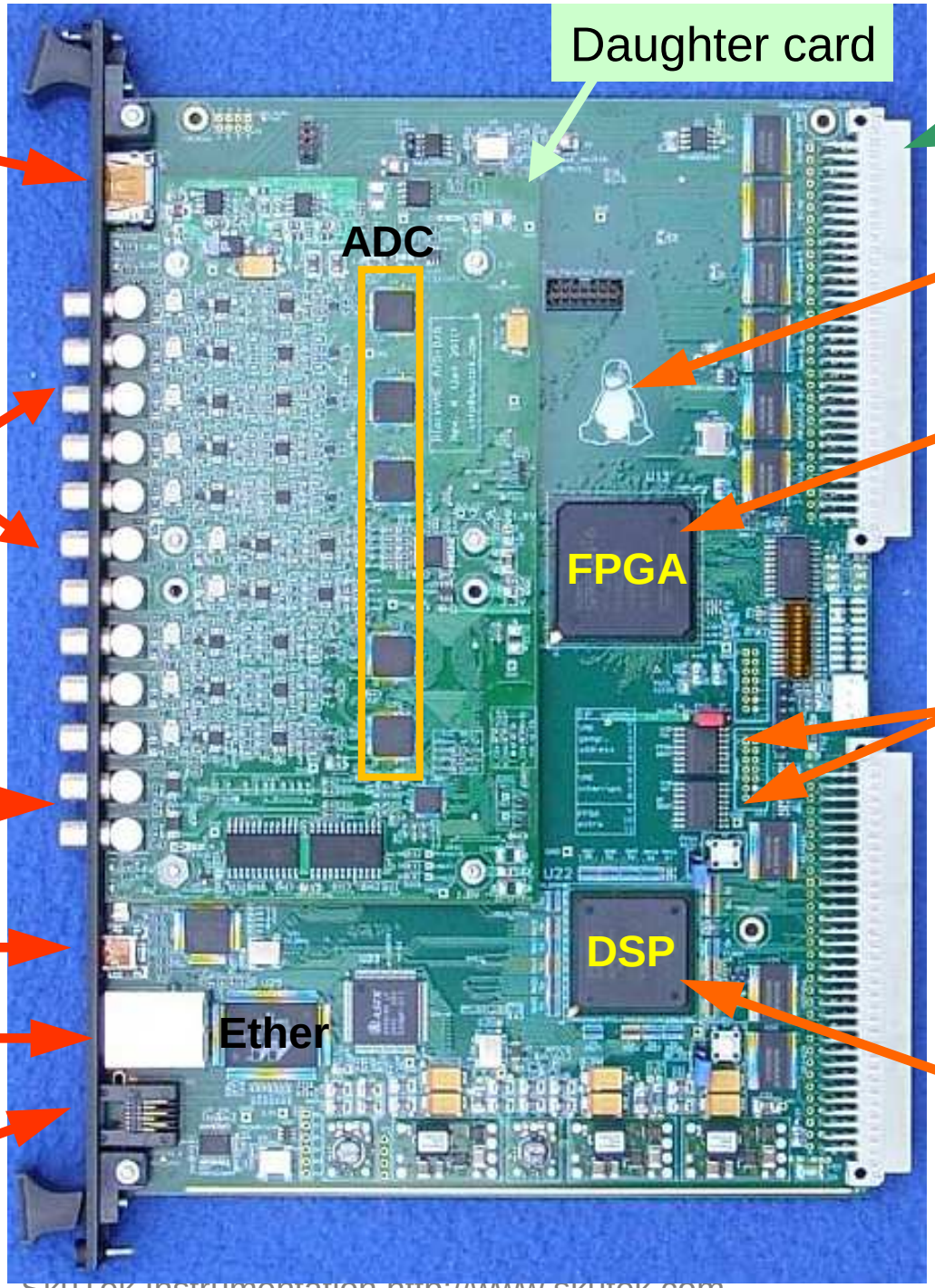
Some other groups would rather procure a complete DAQ system.

Complete DAQ system

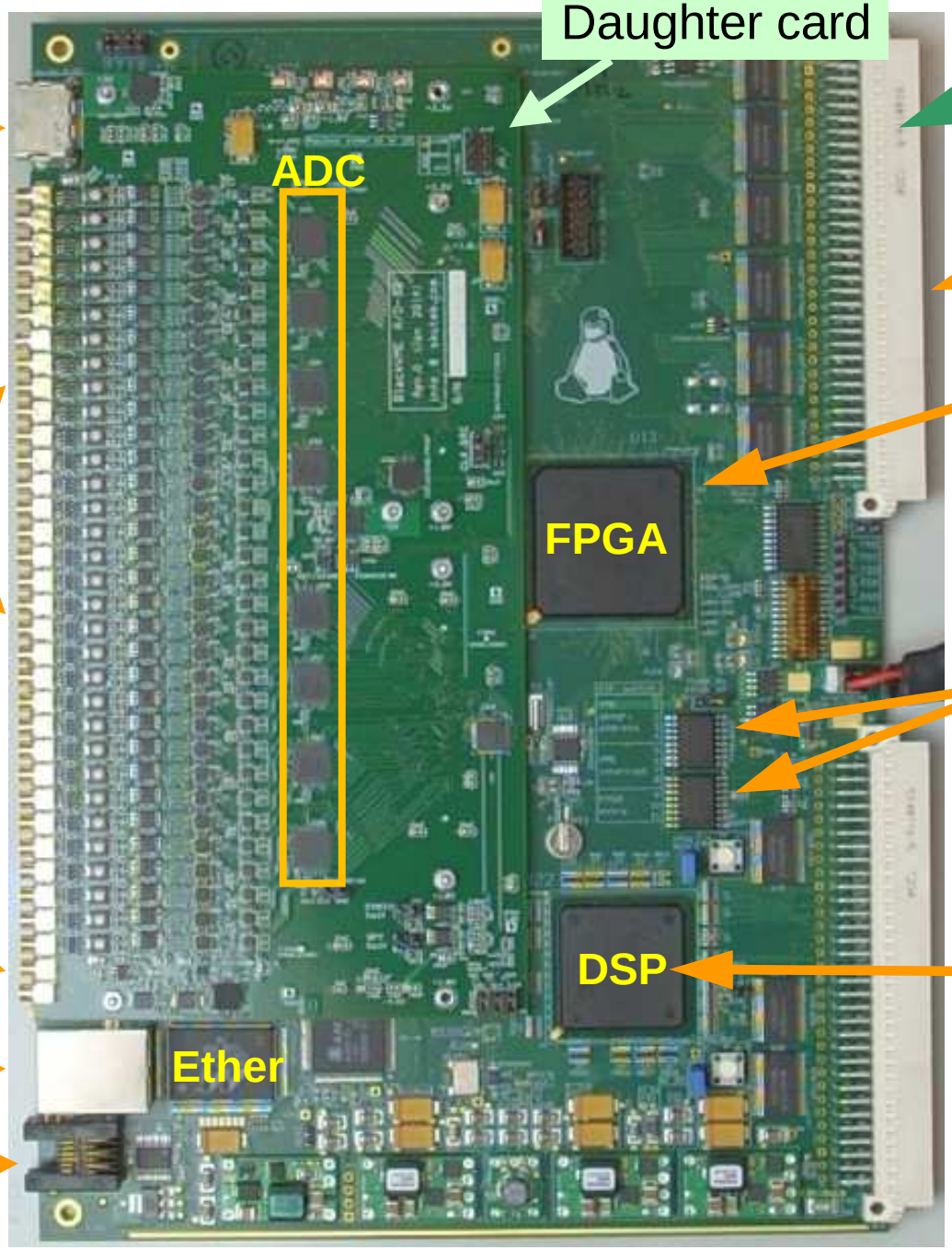
DAQ modules = components



Digitizer DDC-10 = 10 channels, 14 bits, 100 MSPS

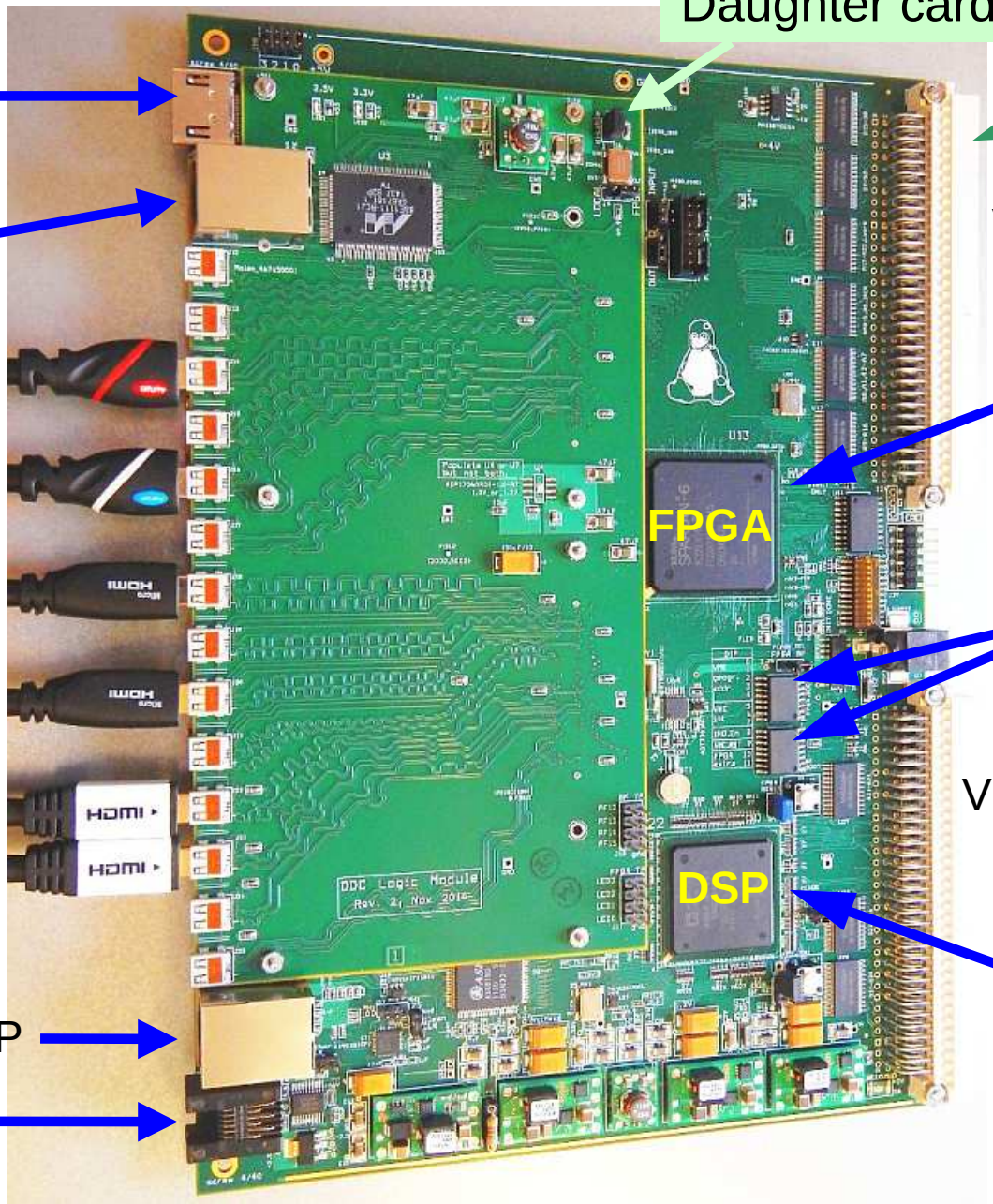


Digitizer DDC-32 = 32-channels, 14 bits, 100 MSPS



Logic Unit: Trigger, Data Readout, ADC Clock, Time Stamp.

This module ties together the DAQ System



Point-to-point link
LVDS SerDes
Data, clock,
time stamp

Full speed GbE
Ethernet from/to
FPGA (direct)

14 * HDMI-D

Ethernet from/to DSP

RS-232

Daughter card

Common motherboard

VME

FPGA

Flash chips:
Linux system
and FPGA
firmware

VME

600 MHz dual-core
processor
ONLINE
PROCESSING

System Architecture

Up to 14
SerDes links:
Data, clock, TS

Data, ADC clock, TS

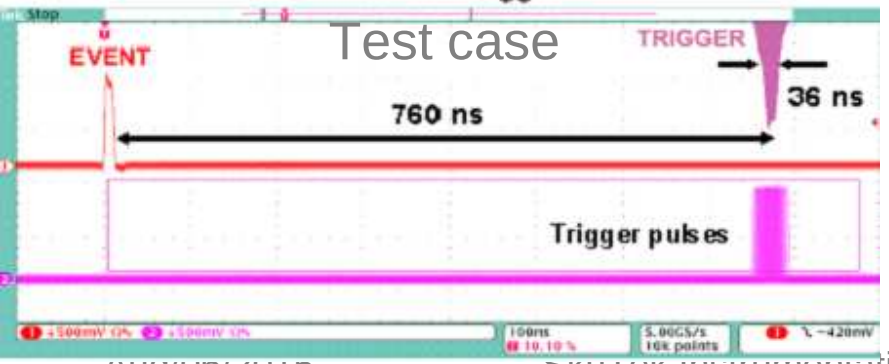
Each link:
1.8 Gbit/s
225 MB/s
as of Jul/24/2015

225 MB/s to the next Logic level

Full GbE speed to Data Recorder

Ethernet for control and monitoring

FPGA Trigger
Test case



Data Collector

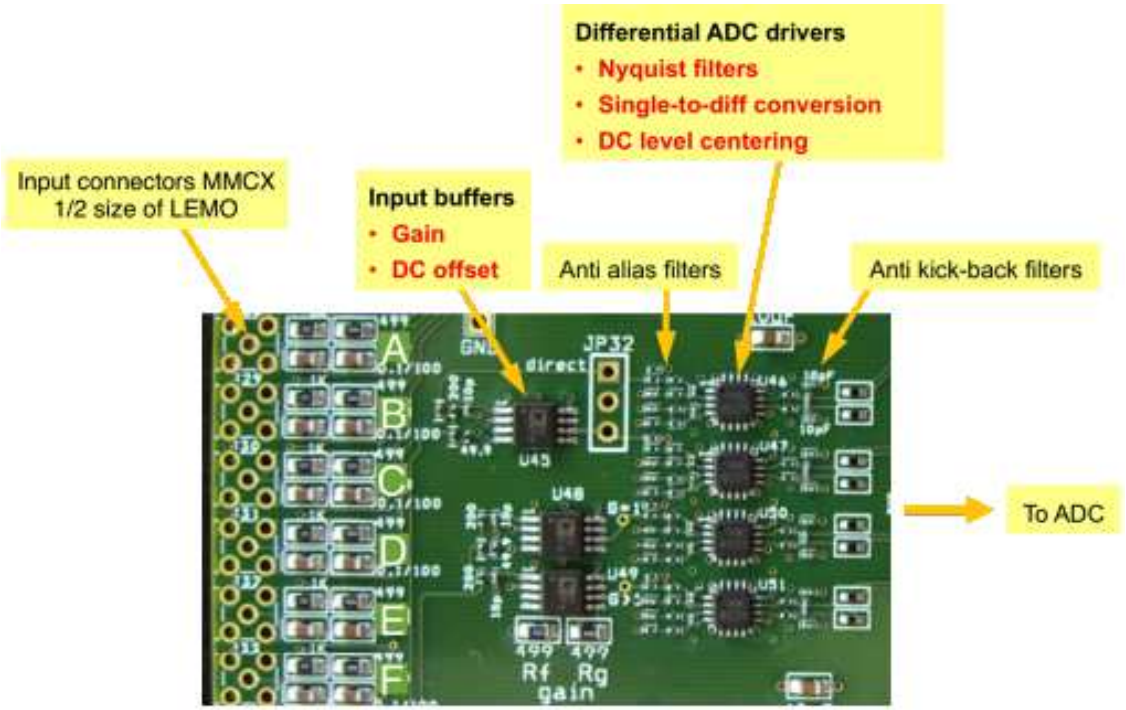
Work by Eryk Druszkiewicz, UofR

Components of the tested Data Collector prototype:

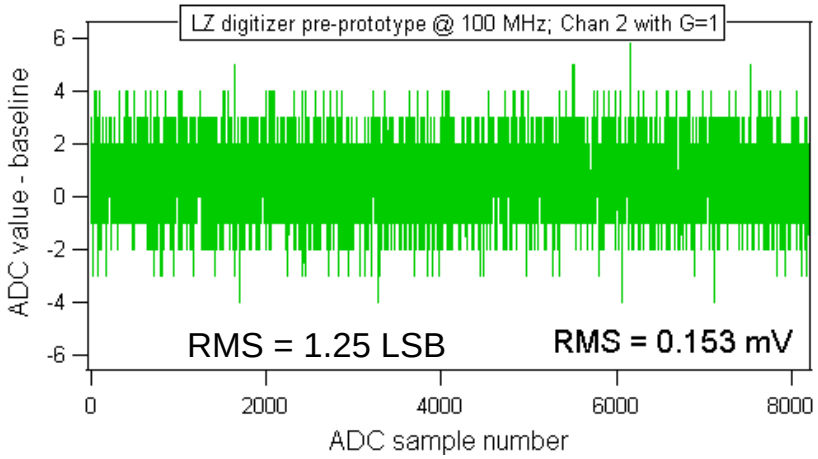
Processor:	Intel Xeon E3-1270V3 3.5GHz Quad-Core	**HDD:**	SAMSUNG 840 Pro Series 256GB SSD
Motherboard:	ASUS P9D-V ATX		Western Digital RE4 4TB 7200 RPM
Memory:	16GB Kingston DDR3 SDRAM ECC	**Case:**	NORCO RPC-270 2U Server Case
NIC:	Intel Ethernet Server Adapter I350-T2	**Hot Swap:**	ICY DOCK 3.5" and 2.5" SATAIII HDD Rack Tray

The Collectors will be built with off-the-shelf components

Performance of a Single ADC Channel



Free run noise waveform.
Digitizer input terminated with 50 ohms.

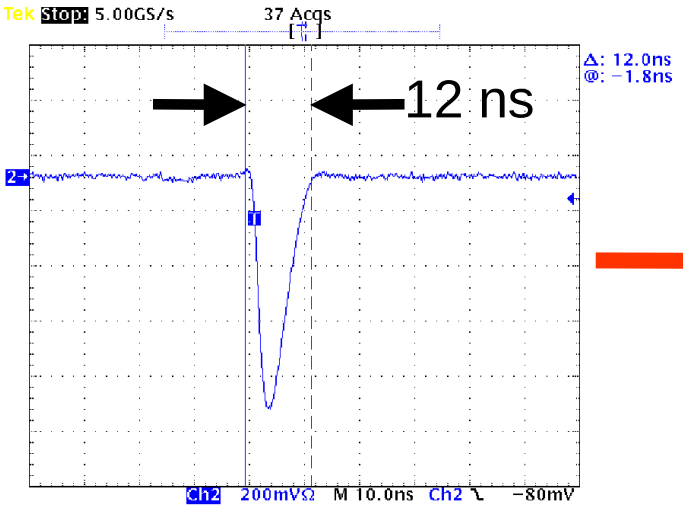


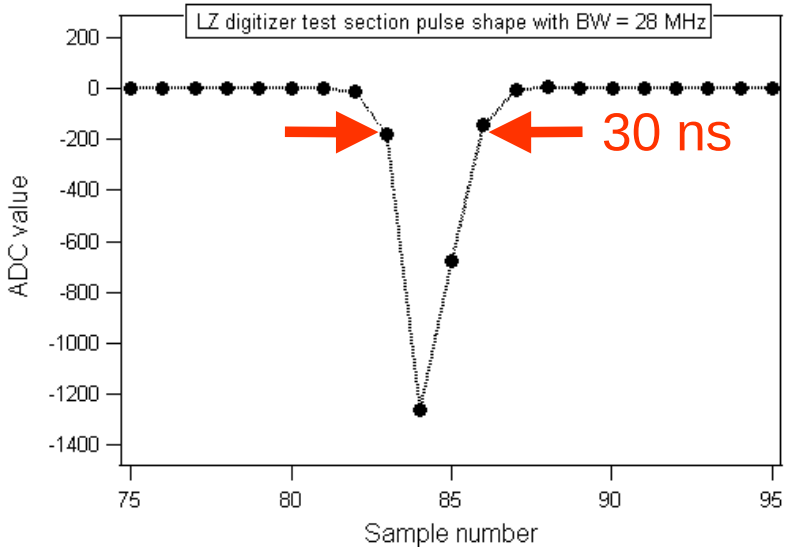
Response to a 12 ns pulse*

*Total width

The on-board anti-alias filter is shaping the input pulses to ensure that even the fastest pulses are digitized with an adequate number of samples.

Similar to PMT pulse





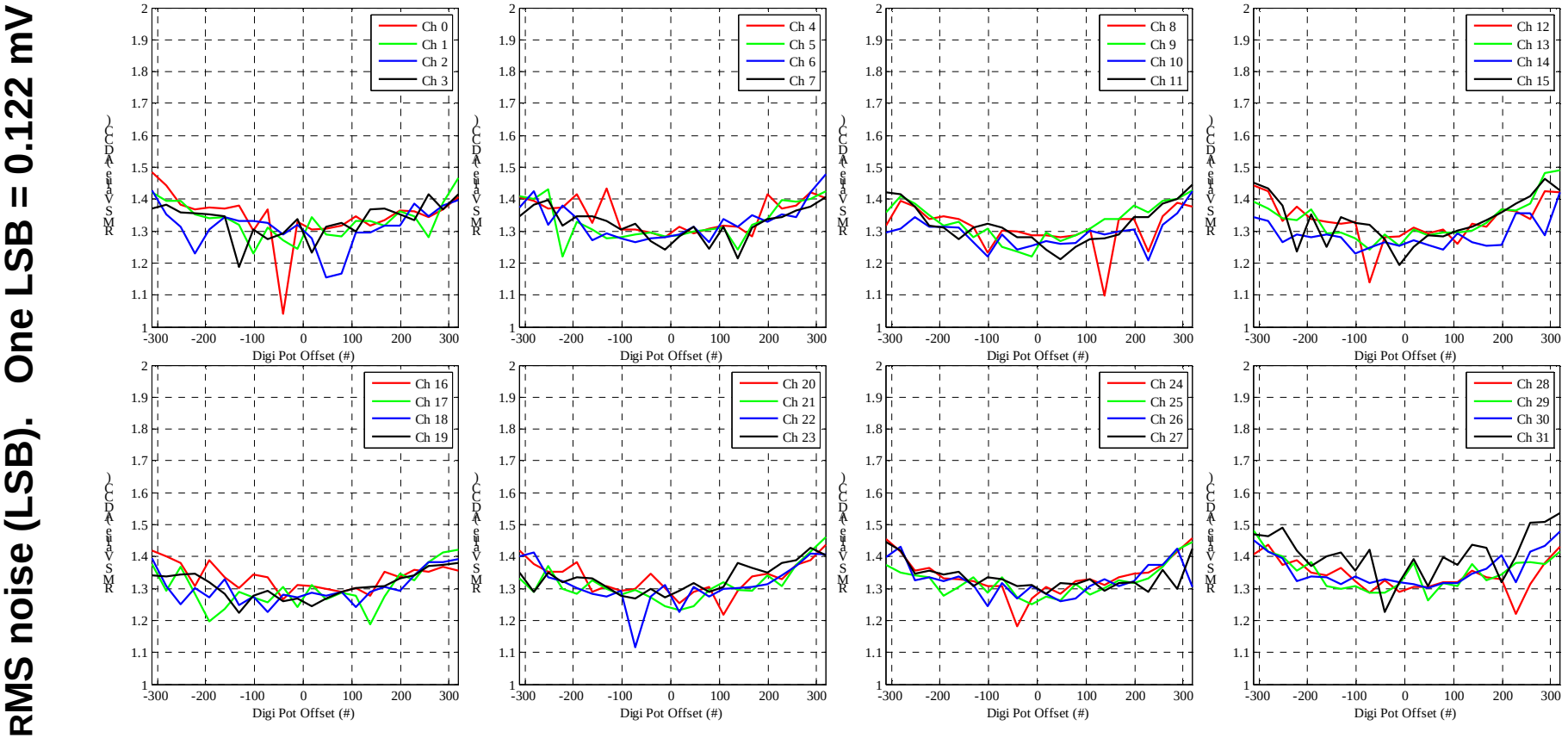
RMS Noise of All 32 Channels (DDC-32)

University of Rochester tested the DDC-32 in preparation for the LZ System tests.

The highlights of the DDC-32 instrument:

Tested and compiled by Eryk Druszkiewicz, UofR

- The RMS noise in all 32 channels is about 160 μV = **1.3 LSB**. There is a very slight dependence on the offset by ~0.1 LSB.
- An on-board digital potentiometer can position the baseline anywhere within the ADC span -1.0V to +1.0V (which is -8k to +8k counts). This will help utilize the entire available ADC range for unipolar pulses.



Baseline offset (a sweep over the entire ADC range = - 1.0 V to +1.0V)

Each point calculated from a 16384 sample long waveform.

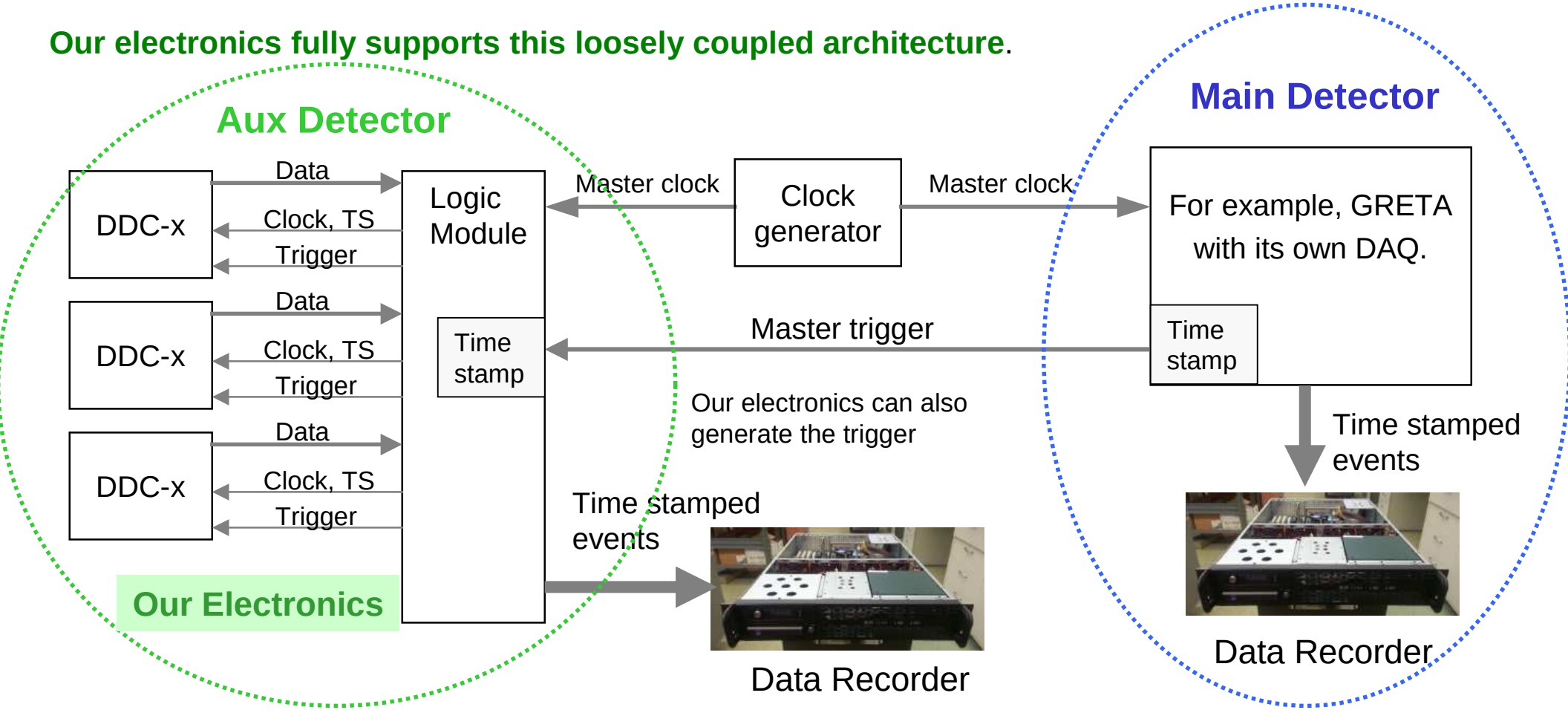
Relevance to the NP program (details)

The recent trend in DAQ architecture is that a *main detector* is operated together with *auxiliary detectors*.

For example, GRETINA + FMA, or Gammasphere + MicroBall.

- The main and auxiliary detectors are equipped with their own DAQs, usually developed by independent research groups.
- The DAQs are loosely coupled. They record separate data streams.
- The final *event building* is performed offline, based on *time stamps*.

Our electronics fully supports this loosely coupled architecture.



Schedule

- High density DAQ modules:
  - **DDC-32**: **32** channels, 14 bits @ 100 MSPS, low noise (available now).
  - **Logic Unit**: 14 LVDS sockets, event preprocessing, triggering, and data streaming (now).
- Low density DAQ modules are available now or will be available this year.
  - **DDC-10 100 MHz**: **10** channels, 14 bits @ 100 MSPS (now).
  - **DDC-10 250 MHz**: **10** channels, 14 bits @ 250 MSPS (this Fall).
  - **DDC-2 100 MHz**: **2** channels, 14 bits @ 100 MSPS, very low cost **<$1k** (this Fall).
- Additional electronic modules, firmware, and R&D, as requested by the community.

Future plans

"Prediction is very difficult, especially if it's about the future." -- Niels Bohr

We plan the following (not necessarily in this order):

- Advance high density digitizers beyond 32 channels per unit.
- Increase the speed of Readout Modules beyond 1 Gb/s.
- Employ faster and more powerful FPGAs and microprocessors.
- Add more kinds of modules to our product line.
- Our plans depend on the reception of our work by the community.

Please tell us what you need, and we will do it for you.

Questions for the NP community

Basically, we have only one question:

What do you need to get developed in order to advance your experimental work?

We will develop it for you!

Thank you for your attention! 

Acknowledgements

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