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Development of High Density Low Cost Readout Modules for Large Scale Radiation Detectors

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Outline



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Company Information



XIA LLC produces advanced X-ray and gamma-ray detector electronics and related instruments with applications in research, industry, and homeland security.

- Located in the San Francisco Bay Area
- ~20 employees
- Products range from 2"x3" OEM circuit boards to 3'x3'x2' detector assemblies, \$500-50,000
- Two main product lines:
 - <u>DGF Gamma ray processors</u> (higher precision, coincidence, waveforms) for HPGe, scintillators, silicon strip detectors
 - <u>DXP X-ray processors</u> (higher throughput, fast mapping) for Si(Li), HPGe, silicon drift detectors

Products Overview



- Replacing analog multi-module electronics with all-digital pulse processing in FPGA and/or DSP.
- Early products were pulse processing modules based on CAMAC standard; now most instruments are based on PXI (or PXIe) standard or are standalone USB devices.



Products Overview





Falcon-X



DXP XMAP



DXP Mercury



Micro-DXP



DXP Saturn



DGF Pixie-500 Express



DGF Pixie-4



DGF Pixie-16

Ultra-LO 1800



PhosWatch



DXP Mercury-4-OEM

Sample Applications



Compact clover readout system with single Pixie-4



HPGe detector array, gamma ray tracking with multiple Pixie-16



SBIR Successes



Agency	Grant Number	Year	r Project Title Award Amount		Sales & Revenue as of 09/30/2012
DOE SBIR	DE-FG03-2ER81311	1992	Digital Processing Electronics for X-ray Detector Arrays	\$550k	~\$2.2m
NIH SBIR	5R44-CA69972-03	1995	High Speed Detector for Mammography Calibration	\$825k	~15.0m
DOE SBIR	DE-FG03-7ER82510	1998	Digital Processors for GRETA Detectors	\$825k	~2.5m
DOE SBIR	DE-FG02-1ER83320	2001	Processing Electronics for Beta- Gamma-Gamma Detection	\$875k	~10.5m
			$\boldsymbol{\zeta}$	\$3.075m	\$30.2m

Other SBIR Projects



Agency	Year	Project Title	Award Amount
DOE SBIR	2013	Proximity charge sensing readout in HPGe detectors	\$150k
DOE SBIR	2011	Silicon Drift Detectors for High Resolution Radioxenon Measurements	\$953k
DOE SBIR	2007	Electronics for Large Superconducting Tunnel Junction Detector Arrays for Synchrotron Soft X- ray Research	\$1m
DOE SBIR	2005	Low Level Radioactive Xenon Monitoring by Phoswich Detector System	\$875k

Motivation



- Large scale nuclear physics experiments with hundreds or thousands of detector channels
 - Existing off-the-shelf readout electronics prohibitively expensive
 - Need for high density, low cost readout electronics with good linearity, timing and energy resolutions
- Recent improvements in the design of commercial ADCs have resulted in a variety of multi-channel ADCs that are natural choice for designing such high density readout modules
 - 4 or 8 channels integrated on a single chip
 - 10 to 16 bits and 40 to 250 MSPS sampling rates
 - Consume power as low as ~50 mW per channel

Large Scale NP Detectors



- **Boo**ster Neutrino Experiment (BooNE) at Fermilab
 - Investigate the question of neutrino mass by searching for oscillations of muon neutrinos into electron neutrinos
 - MiniBooNE, the first phase of BooNE, uses a single detector which is a large tank of 800-ton mineral oil liquid scintillator and viewed by 1280 photomultiplier tubes ⇒ >1280 readout channels needed
- Absolute Luminosity For ATLAS (ALFA)
 - Each detector module consists of ten layers of two times 64 scintillating fibers each
 - The fibers are coupled to 64-channel Multi-Anodes PMTs
 - The total number of channels is about 15000
- GRETINA, the first stage of a full Gamma-Ray Energy Tracking Array (GRETA)
 - A large number of auxiliary detectors are planned for GRETINA,
 e.g. silicon and scintillation particle detectors and gas counters

Multi-channel ADC Specs



Parameter	AD9222	ADS6425	AFE5801	AD9432
Bits	12	12	12	12
Channels	8	4	8	1
Rate	65 MSPS	125 MSPS	65 MSPS	100 MSPS
Input voltage (diff. swing)	2 Vp-p	2 Vp-р	2 Vp-p	2 Vp-р
VGA	No	No	Yes	No
AAF	No	No	Yes	No
INL (max, LSB)	± 1.0	± 2.5		± 1.0
INL (typ, LSB)	± 0.4	± 1.0		± 0.5
DNL (max, LSB)	± 0.65	+2.0/-0.9		± 0.75
DNL (typ, LSB)	± 0.3	± 0.5		± 0.25
ENOB	11.38	11.4		11.0
Power/channel	114 mW	325 mW	58 mW	850 mW
Supply voltages	1.8V	3.3V	1.8V, 3.3V	3.3V, 5V
RMS noise	0.27 LSB	0.407 LSB		

SBIR Project Objectives



SBIR Project objective is to develop a high channel count, low cost, and versatile digital readout module for large scale nuclear physics radiation detectors

- Pixie-32": a 32-channel digital gamma-ray spectrometer
- target price per channel will be only \$200-\$300 while it will still be a true spectrometer
- Implement a PCI Express interface (up to 1 GB/s) on Pixie-32 modules (versus the regular 100 MB/s PCI interface on Pixie-4 and Pixie-16)

Technical Approach



SBIR Phase	Tasks	Status
I	Verify capability of modern FPGAs to receive Gbit/s data streams from a multichannel ADC	Done
I	Estimate costs for differed board architectures	Done
I	Verify multichannel ADCs for spectroscopy quality	Done
II	Finalize architecture for the Pixie-32 spectrometer	Done
II	Draw design schematics and layout printed circuit boards	Done
II	Manufacture a small number of prototype boards	Done
II	Develop Pixie-32 FPGA firmware	In Progress
II	Develop PCI Express driver and API library	In Progress
II	Develop a use interface that can be used for 100's or even 1000's of data acquisition channels	Starting







HPGe energy resolution (keV, FWHM)

Energy (keV)	AD9222		ADS6425		AFE5801		
	Ch0	Ch1	Ch0	Ch1	Ch0	Ch1	AD9432
122	0.92	0.92	0.98	1.08	1.15	1.16	0.84
661.6	1.34	1.36	1.36	1.43	1.55	1.55	1.28
1332.5	1.78	1.80	1.84	1.82	1.96	1.96	1.72
2614.5	2.39	2.44	2.47	2.52	2.64	2.63	2.36



Energy spectra from a 1"×1" cylindrical LaBr₃ crystal coupled to a 2" PMT irradiated with ¹³⁷Cs



DOE SBIR/STTR Exchange Meeting, Nov. 6-7, 2013, Washington, D.C.







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Differential Nonlinearity (DNL) Tests of Multichannel ADC



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Timing resolution measured using a single LaBr₃/PMT detector and a ¹³⁷Cs source. The output of the LaBr₃/PMT was split into two branches and then fed into two ADC channels.







8-Channel Variable-Gain Amplifier (VGA) With Octal High-Speed ADC

Eight Variable-Gain Amplifiers (VGA)
 Variable Gain, –5dB to 31dB With 0.125dB or 1dB Steps
 Digital Gain Control

Third-Order Antialiasing Filter With Programmable Cutoff Frequency (7.5, 10, or 14MHz)

✦Analog-to-Digital Converter (ADC)
 ➢ Octal Channel, 12Bit, 65MSPS

Pixie-32 Architecture





Pixie-32 System Diagram





Pixie-32 Block Diagram





Pixie-32 Prototype





Pixie-32 Prototype







Pixie-32 Prototype



32 single-ended analog signal inputs to the Pixie-32 front panel

Phase II Remaining Tasks



- Develop Pixie-32 FPGA firmware
 Real time pulse processing, PCIe communication
- Develop PCI Express driver and API library
 Integrate with XIA's Handel software library
- Develop a user interface that can be used for 100's or even 1000's of data acquisition channels
- Characterize Pixie-32 performance
- Test Pixie-32 at collaborating laboratories

Summary & Outlook



- Characterized spectroscopy performance of multichannel ADCs
- Finalized Pixie-32 board architecture
- Designed and manufactured Pixie-32 prototype boards
- Working on firmware and software for the Pixie-32
- Ongoing efforts to commercialize Pixie-32 as early as possible