ALPHACORE

Analog, Mixed Signal & RF Electronics

Radiation-Tolerant High-Speed Camera

Contract # DE-SC0013232

DOE NP SBIR/STTR Exchange Meeting
August 7-8, 2018
Washington DC

Outline

- About Alphacore
- Program info
- Introduction to radiation effects in image sensors
- High-speed camera architecture and first prototype implementation
- Future plans
- Summary

About Alphacore

- Founded in 2012 and located in Tempe, Arizona
- Providing technologies that enable major advances in:
  - Homeland Security
  - Defense
  - Aerospace
  - Scientific Research
  - Medical Imaging

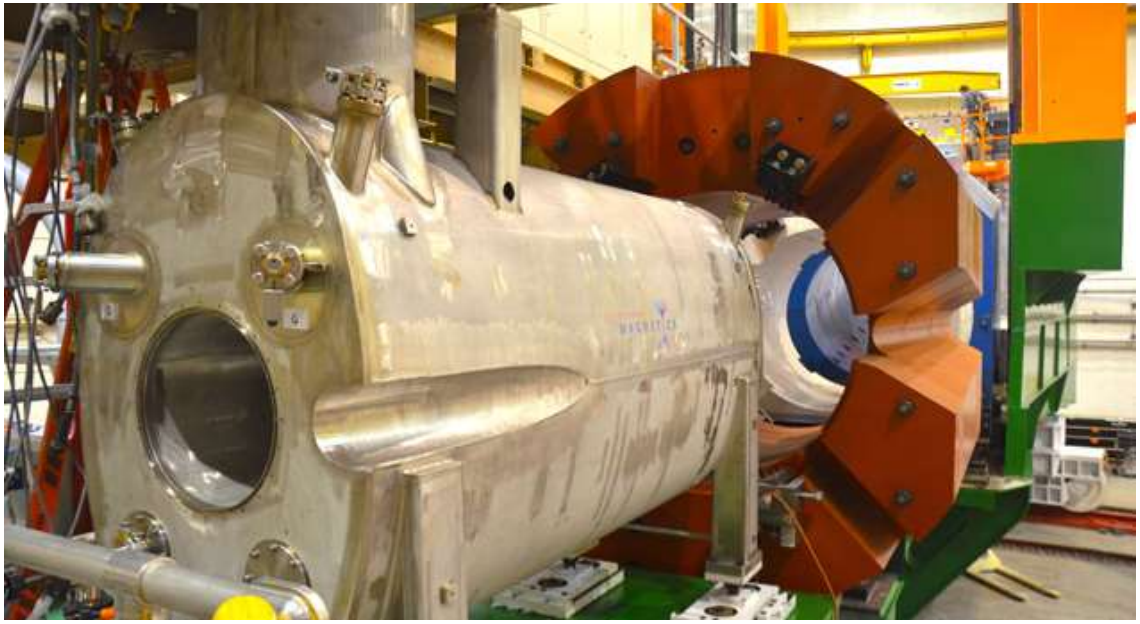
- Product areas span:
  - High performance analog, mixed signal, and RF electronics
  - High-speed visible light and infrared camera systems
- Rapidly Growing

Program Info

DOE SBIR Phase II Contract #DE-SC0013232

DOE need:

A radiation-tolerant, triggerable, **high speed imaging chip and a complete camera system** for investigating rapidly occurring phenomena in radiation environments. The primary applications are beam monitoring and scientific experiments at nuclear physics facilities.



Motivation

Non-hardened image sensors and cameras typically do not operate beyond few tens of kilorads

Hardened sensors and cameras typically target nuclear plant monitoring applications and have low frame rates (30fps)

High-speed rad-hard image sensors and cameras do not exist (to the best of our knowledge)

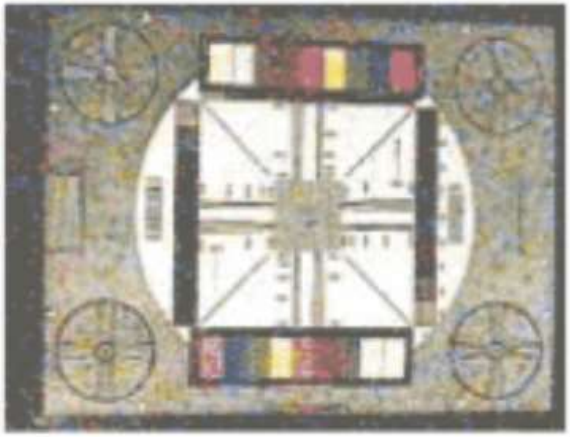
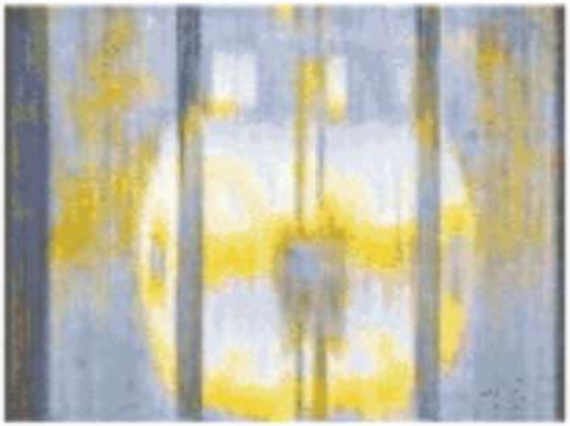


Image before irradiation



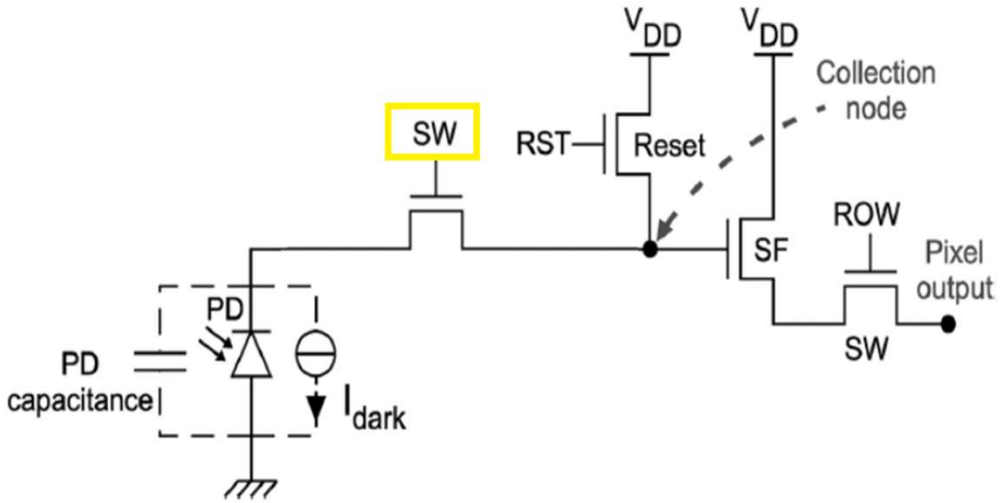
…and after 10krad

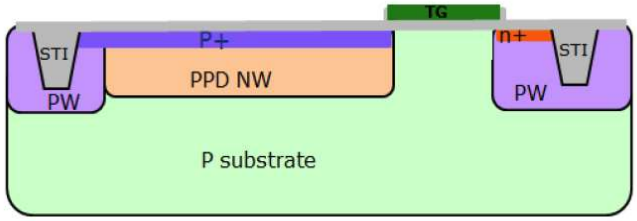
[Courtesy: Vision System Design]

Camera Specifications

Specification	Description
Resolution	Minimum: 10 kilopixels Objective: 1 Megapixel
Frame rate	Minimum:1 kfps Objective: 10 kfps
ADC resolution	10 bits *Dynamic range increased with a programmable gain amplifier*
Pixel	20 µm x 20 µm pixel size 65% fill factor
TID tolerance	Minimum: 100 krad Objective: 300 krad

4T Pixel Topology

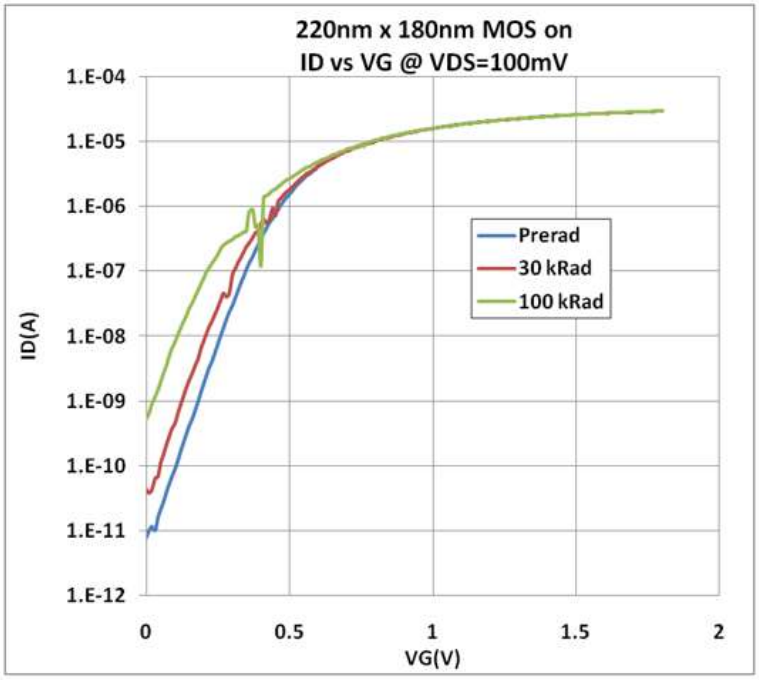




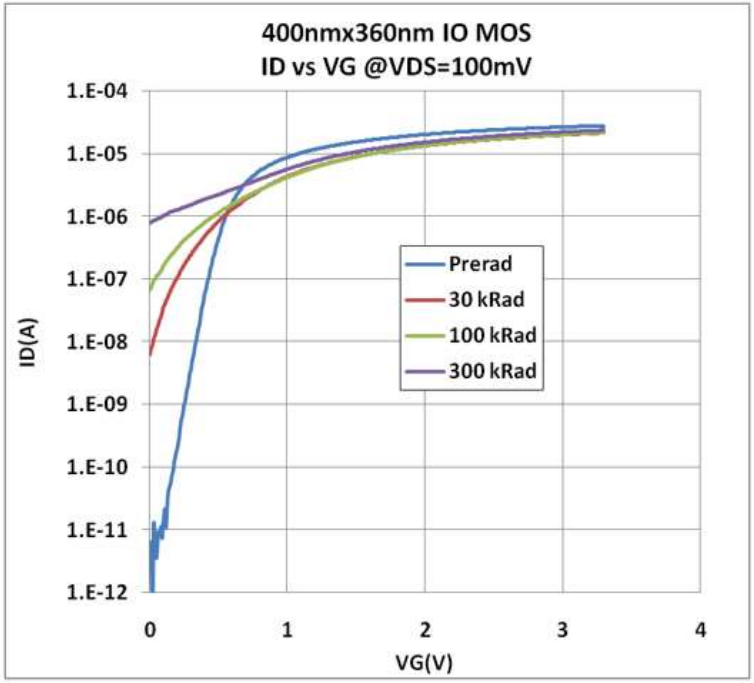
- 1 Megapixel sensor uses 4T pixel topology, Pinned Photodiode (PPD) light-sensitive element
- The pinned photodiode structure uses a shallow p+ layer on top of an n-well layer of a traditional pn junction photodiode. The n well is “sandwiched” between the p+ layer on top and the p epi layer underneath
- A transfer gate is shown as an additional switch (SW), and the collection node is an n+ in p-well floating diffusion
- The PPD is ideal for low light or high-speed applications, such as this DOE program
- Advantages of the PPD and 4T pixel include inherent noiseless gain from PD to the floating diffusion, fast integration and readout times, reduced dark current, lower noise, and increased quantum efficiency

180nm CMOS 1.8V vs. 3.3V NMOS Leakage Due to TID

Min. size 1.8V core NMOS



Min. size 3.3V NMOS in the process

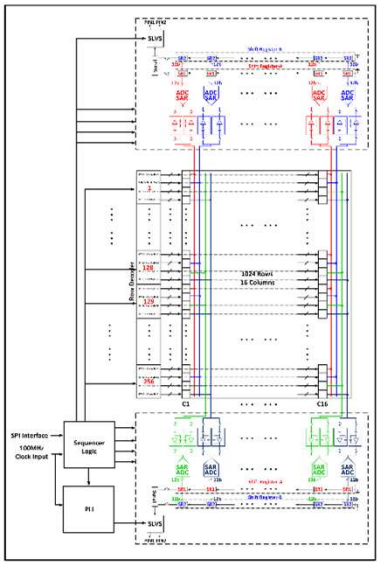


Based on Co-60 tests, the thick oxide NMOS has 100X higher leakage than the core NMOS => Design with 1.8V core transistors

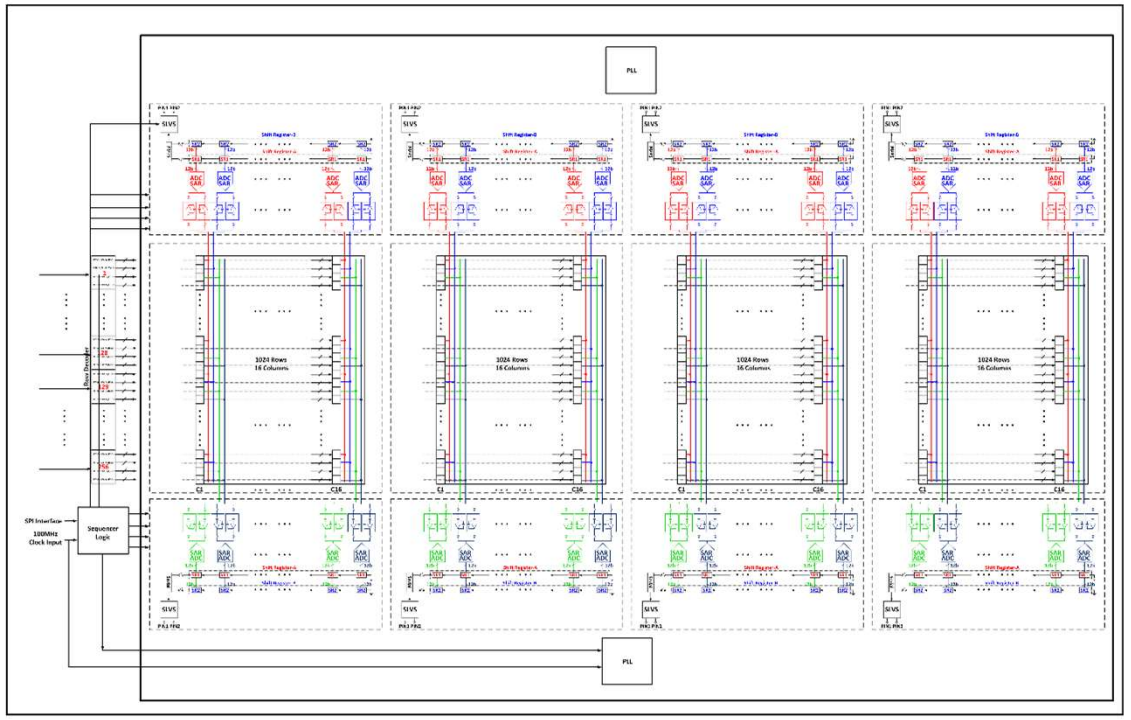
Phase II

- Full 1 Megapixel, 10 kfps chip under development
- Radiation-tolerant design using thin-oxide 1.8V devices for all analog and digital supporting circuits
- Radiation-tolerant pixel design using central T-gate to reduce STI and annular NMOS devices for pixel transistors
- 4 ADCs per column with pipelined data flow (4096 ADCs / chip)
- 12-bit SAR column ADC with 10 µm layout pitch
- Complete solution with on-chip row decoder, digital serial peripheral interface (SPI), control pulse generation, PLL, PGA's, ADC's, biasing, high-speed serializer, low-power scalable low voltage signaling (SLVS) interface
- Radiation tolerant supporting sensor electronics for full radiation tolerant camera solution

Modular 1 Megapixel Sensor Architecture



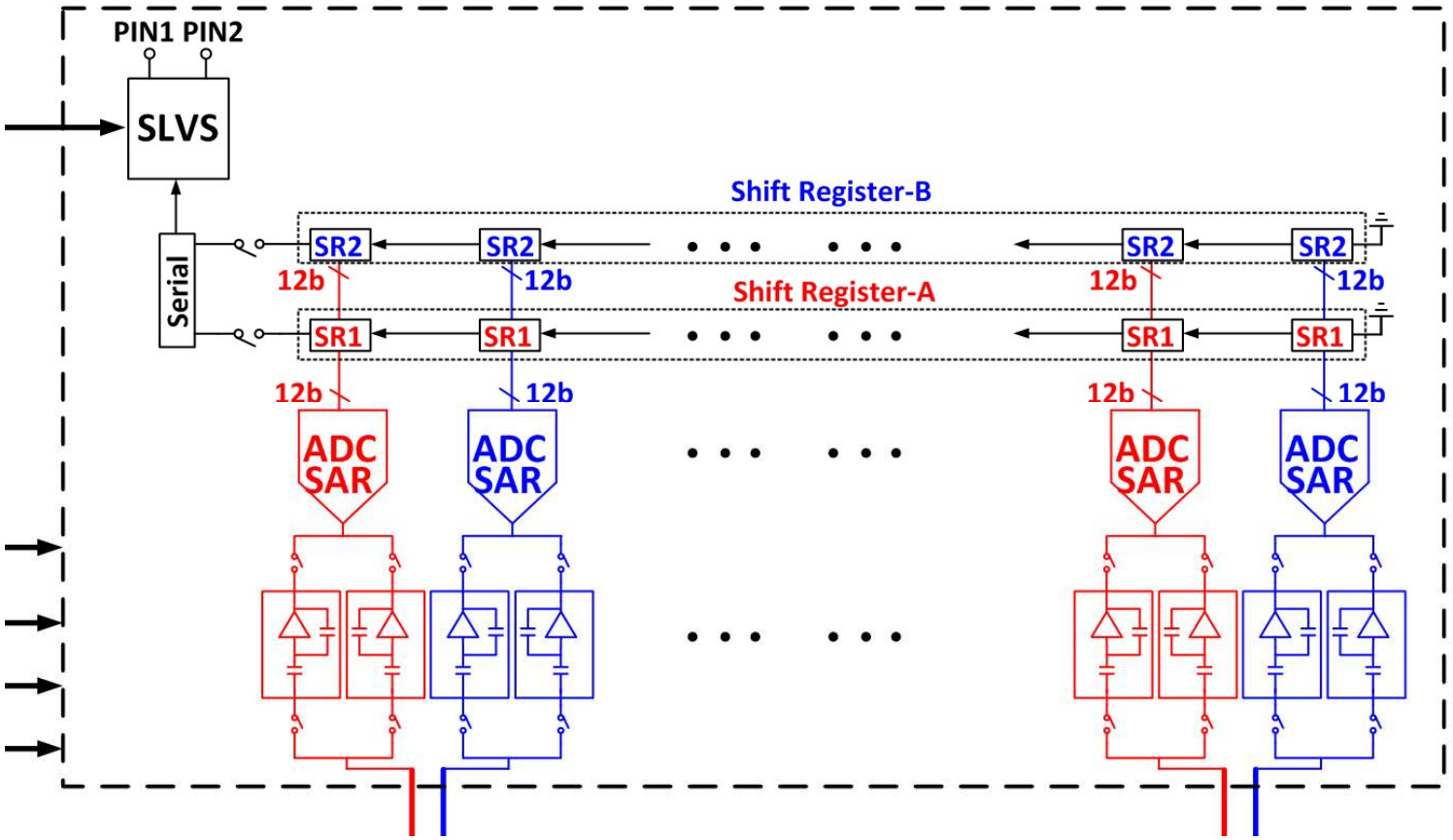
“sub-slice”



“full-slice”

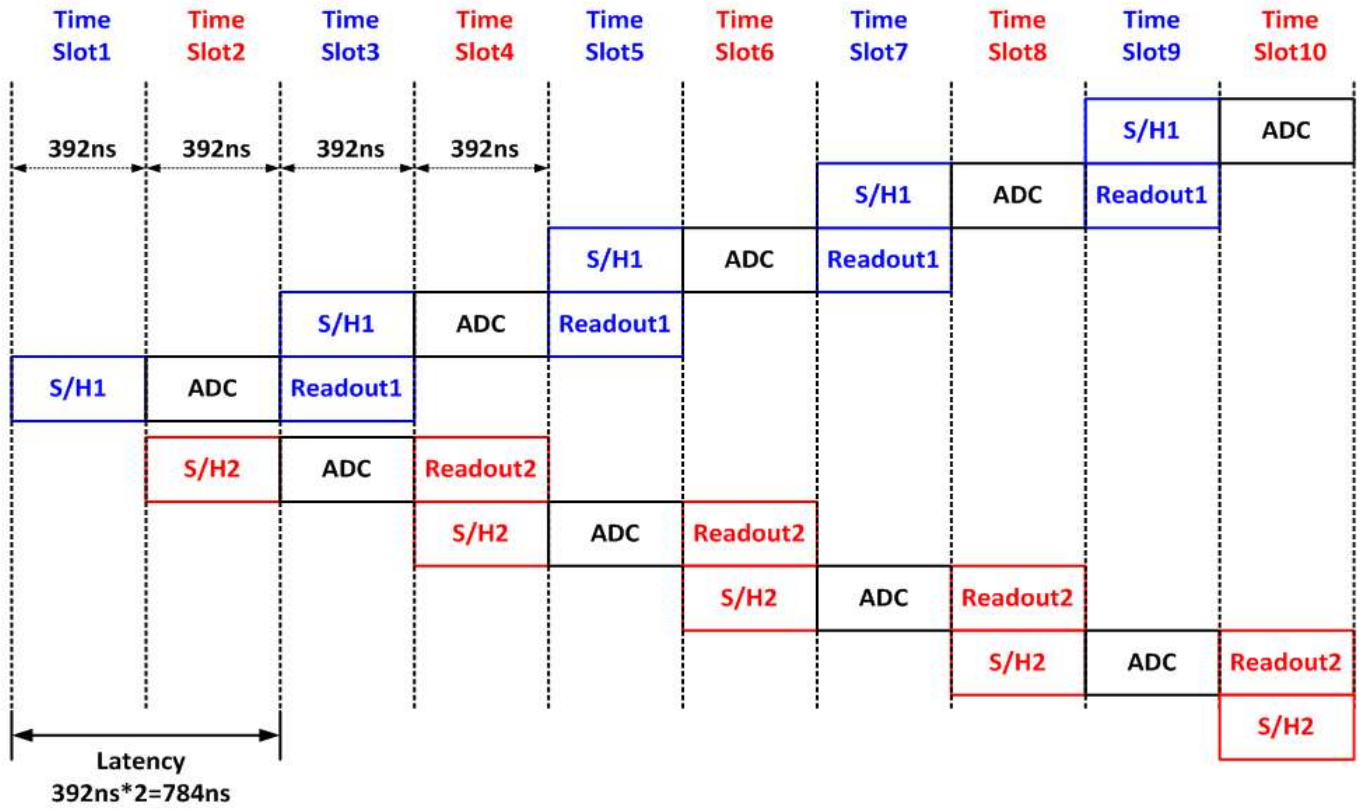
Structure	Summary	Details
Sub-slice	Basic unit	1024 px rows X 16 px columns + 2 SLVS ports
Full-slice	4 sub-slices	1024 px rows X 64 (4x16) px columns + 8 (4x2) SLVS ports
1 Mpx chip	16 full-slices	1024 px rows X 1024 (16x4x16) px columns + 128 (16x4x2) SLVS ports

Pipelined PGA, ADC, Readout



- 2 PGA sample-and-holds per ADC, plus 4 ADCs per column (two top, two bottom)
- Allows pipelined sampling, conversion, and readout.

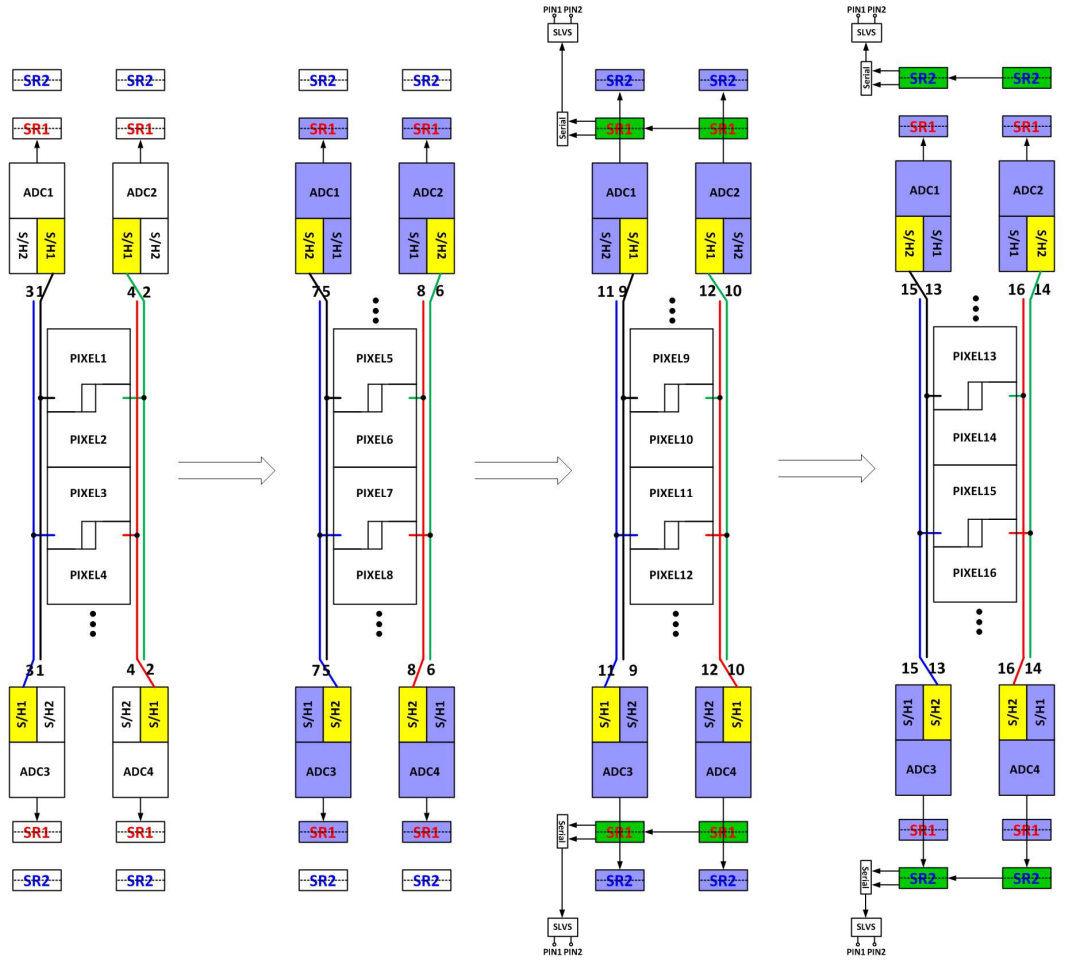
Column Readout Pipelining



The column readout process has 784ns latency before getting digital bits out.
Then each time slot has three operations: one sample and hold, one adc process, and one readout process

Readout uses novel serializer approach where parallel ADC data is latched to a shift register and thereby ready for high-speed serial transfer at the end of a conversion

Column Readout Architecture



- High-speed 1 Gbps readout architecture
- Pixel values sampled onto PGA
- A to D conversion starts while next pixels are sampled
- Parallel A to D result is shifted out at 1Gbps DDR
- 500 MHz clock generated with on-chip PLL
- SLVS interface has 200 Ohm effective termination and 400 mV supply vs. 50 Ohms and 1.8 V for LVDS → large power savings

Radiation Tolerance Strategy: I/O Transistors

Direct action has been taken (simulation, schematic & layout):

Corner Simulation with dV_{th} of >100mV (NMOS and PMOS)

1 Mrad (SiO_2) target (see previous slide)

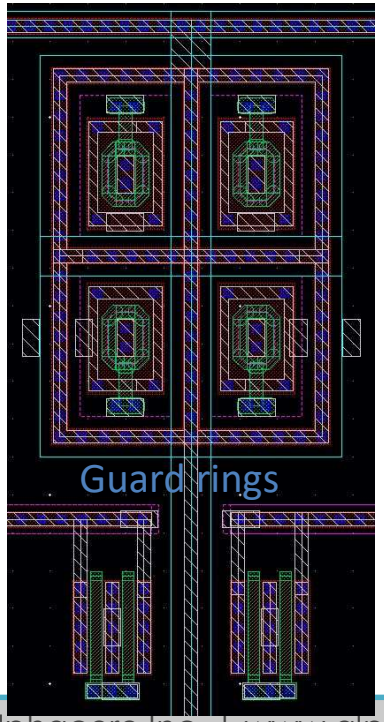
Enclosed NMOS transistor

- Avoid STI leakage path

Guard rings

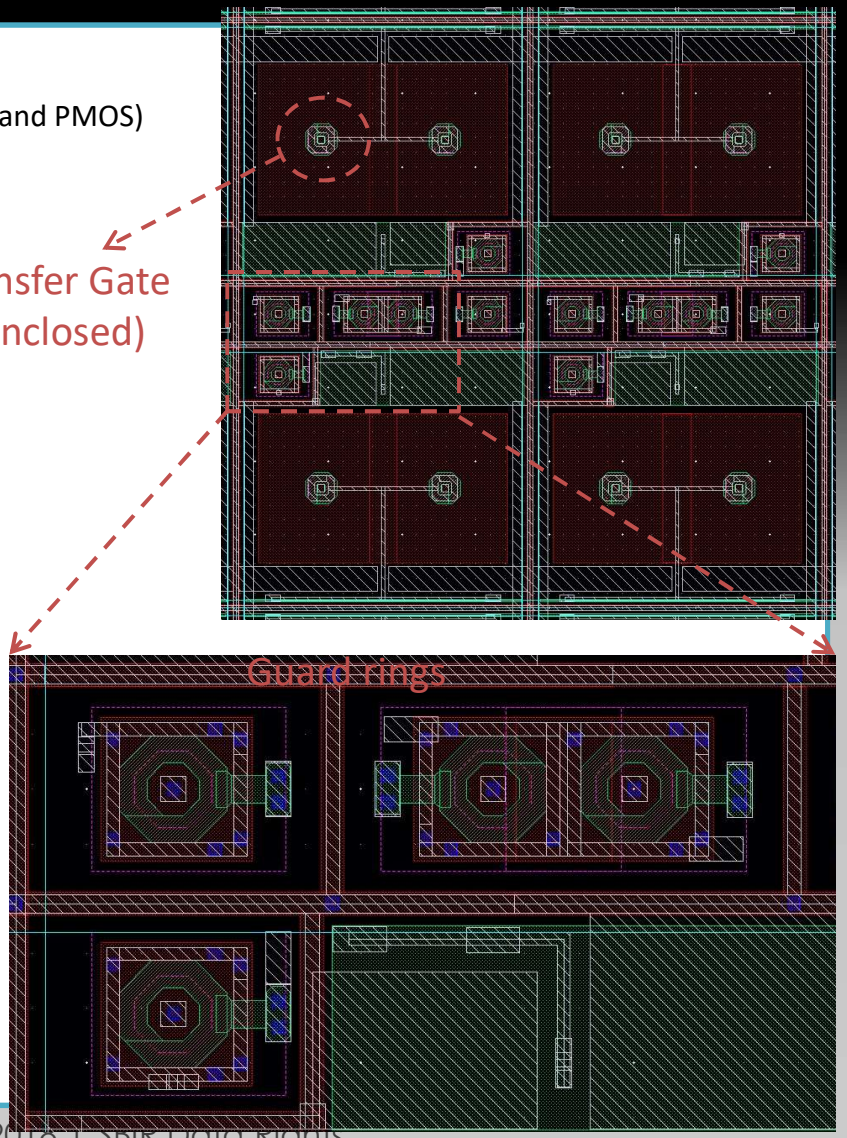
- Prevent leakage between transistors

Column Layout



- Annular NMOS devices used for pixel transistors
- Pinned Photodiodes (PPD) offer inherent conversion gain (40µV/e-) ideal for low light, high speed application
- 20µm by 20µm pixel
- Annular transfer gate on the PPD reduces STI and increases radiation tolerance
- Fill factor of 60-65%
- Very fast transfer time of 170 ns or better

Pixel Layout

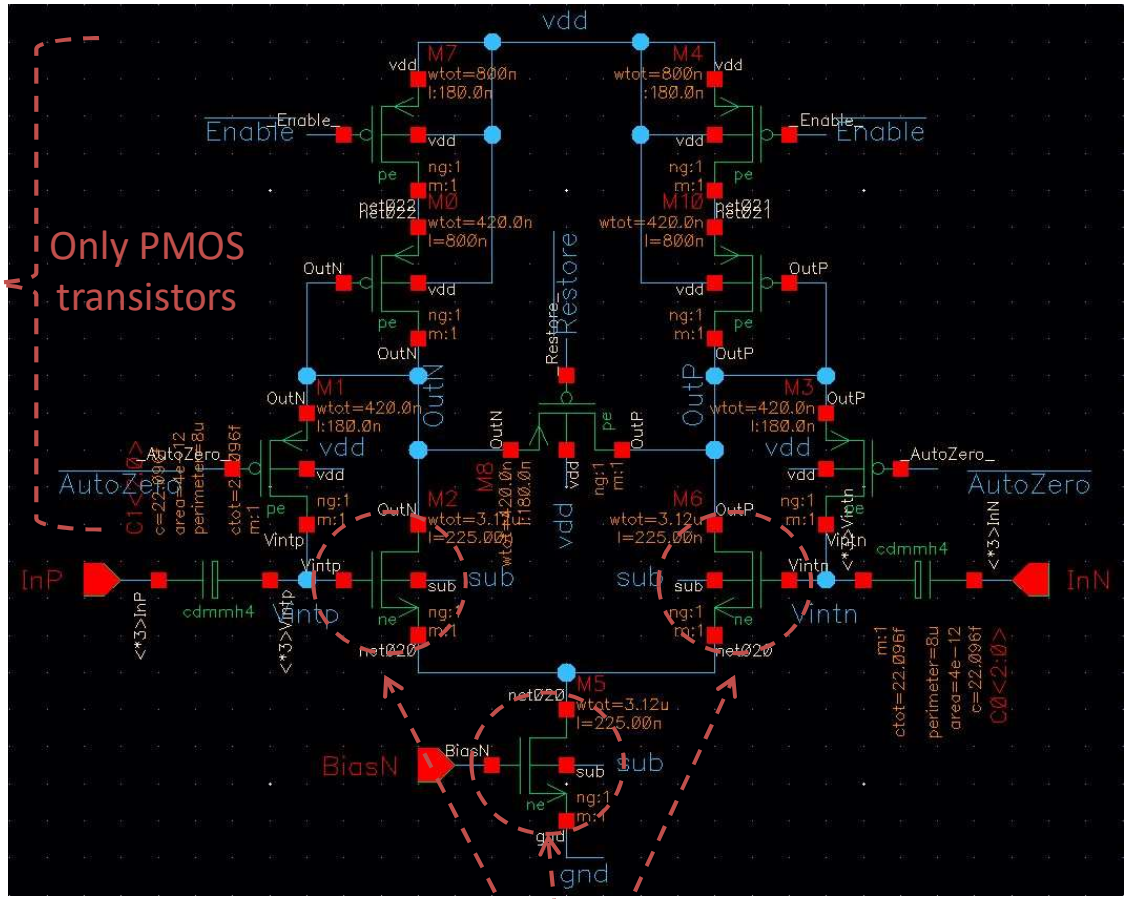


Radiation Tolerance Strategy: Core Transistors

Design provision has been made to enclose NMOS transistors in a sensor re-spin if necessary:

- No need for DV_{th} corner Simulation
  - Naturally very radiation tolerant (see first slide)
  - Only few millivolt shift
  - >>1 Mrad (SiO_2) target
- Enclosed NMOS transistor ready
  - NMOS size adequately chosen in schematic
  - Easy sensor re-spin with no re-design
- Effort to keep the design mostly PMOS-based
  - No need of enclosing the device
- Guard rings added in layout
  - Prevent leakage between transistors

Example of schematic using core transistors:



Radiation Tolerance Strategy

Process used for this design has two types of transistors:

- Core transistors
  - Used almost everywhere (~90% of the transistor population)
  - 0.18mm process
  - Power supply of max 1.8V
- I/O transistors
  - Used where >1.8V supply is needed (pixel, column…)
  - 0.35u process
  - Power supply of max 3.3V

Oxide thickness (t_{ox}) is ~2% of the process node:

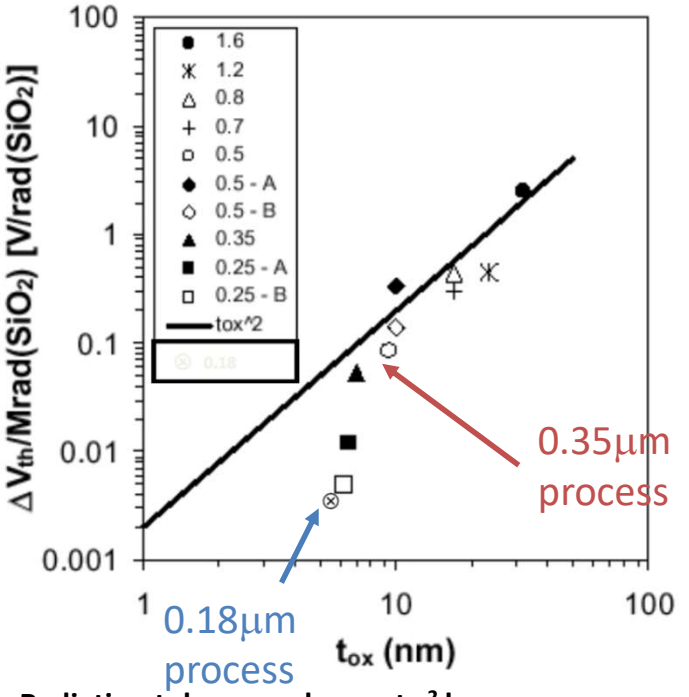
~8nm for 0,35mm process and ~4nm for 0.18mm process

Radiation tolerance depends directly upon t_{ox}

Strategy:

Special attention (layout) has to be paid for I/O transistors

Provision (schematic) has to be made for core transistors

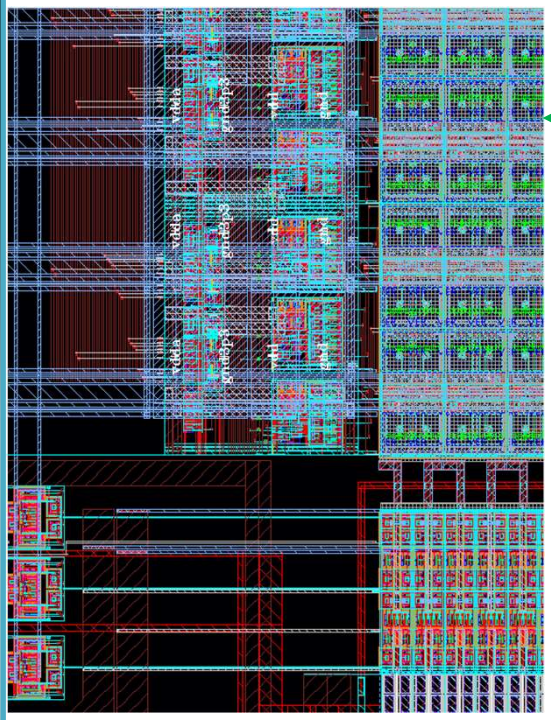


Radiation tolerance obeys a t_{ox}^2 law

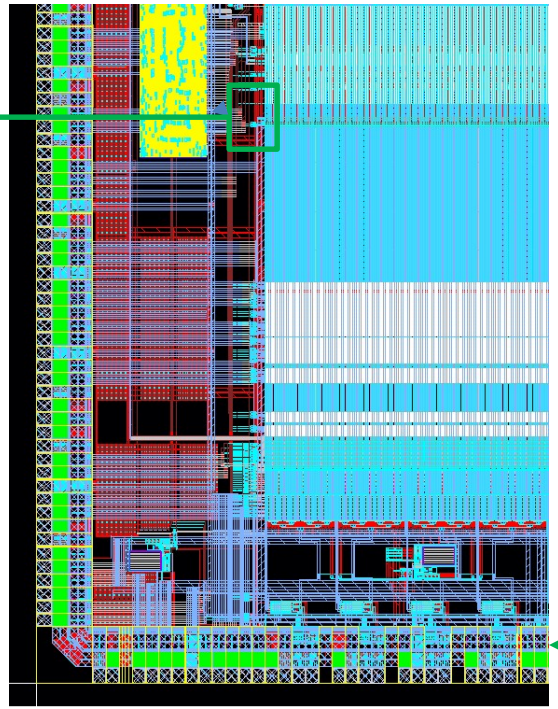
➔ 0.18mm process "naturally" more radiation tolerant than 0.35mm process

From 0.25mm down, tunneling effect kicks in (departure from the t_{ox}^2 law) and further help the smaller node process radiation tolerance

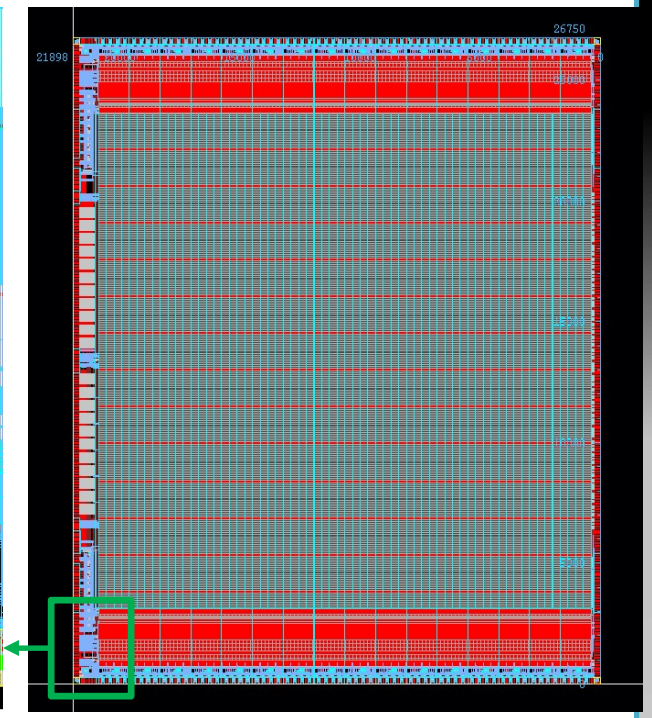
Rad-Hard Image Sensor



Zoomed in view of pixels array connection of columns to column bias and row decoders.



Zoomed in view of lower left corner showing pixels, column ADC's, digital controls, PLL, serial readout, and SLVS.



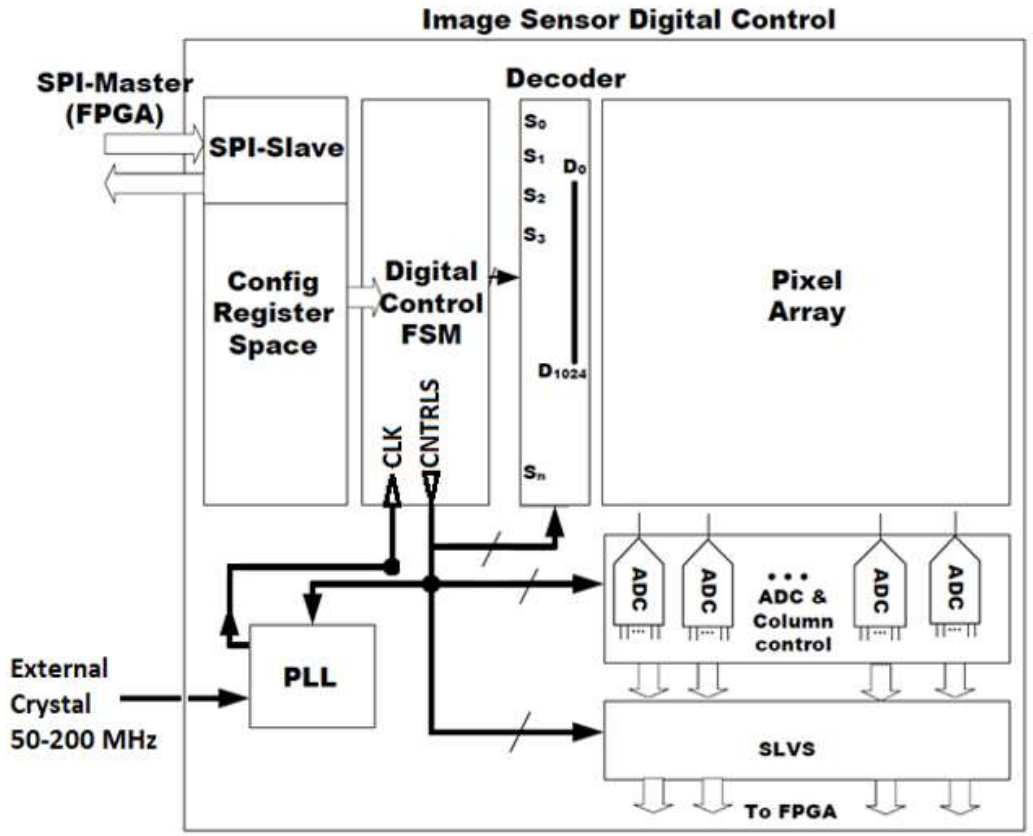
Layout of full 1 Mpixel chip, 27 mm by 22 mm

Radiation Tolerance Strategy: Digital Controls

Configuration registers for digital controls are triple mode redundant.

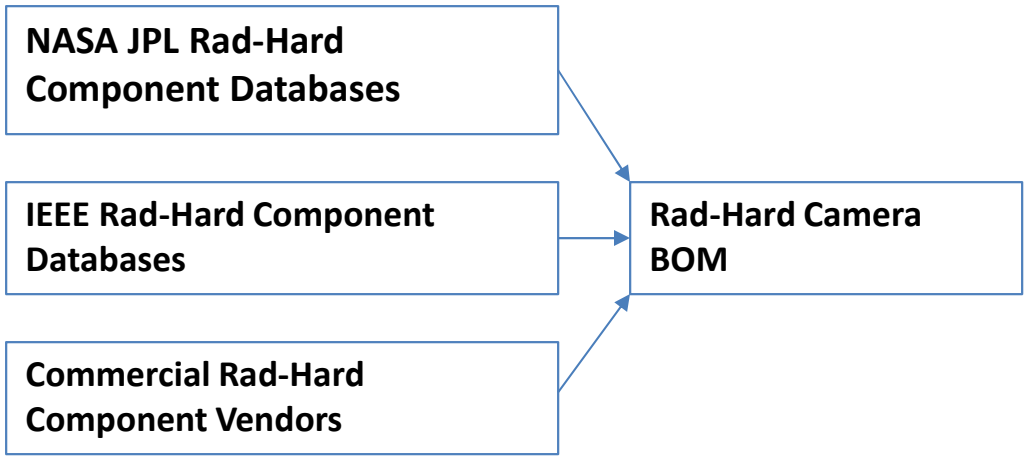
Final revision of the image sensor, logic will be synthesized using a custom rad hard digital library designed to be used with the synthesis and place and route flow.

Control registers can be refreshed through a SPI write if there is an upset.

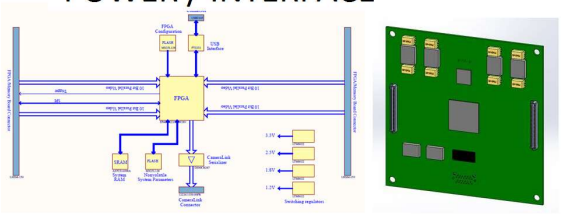


Radiation-Tolerant Camera Electronics

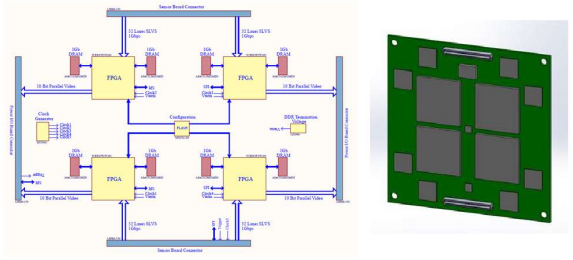
- Camera electronics are modular with pluggable boards for sensor, FPGA, and power/interface
- Interface boards to support multiple protocols (e.g., Camera Link, USB3, GigE Vision)
- Leveraging databases and commercial vendors to create a rad-hard component BOM
- System architecture uses 4 FPGAs and 8 memories to achieve 10 kfps in burst mode



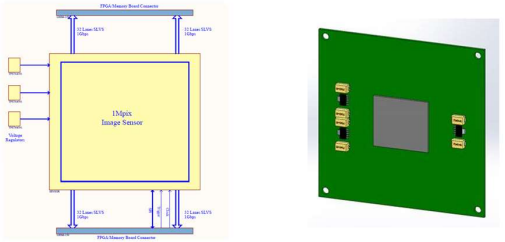
POWER / INTERFACE



FPGA / MEMORY



SENSOR



Future Plans

- Radiation-hardened camera boards
  - Identify tested components
  - Use qualified components where possible
- Camera-Link frame grabber and GUI
- TID tests for the image sensor
- Field test at Jefferson Lab
- Upgrade the camera to be compatible with space applications
  - Single event effects and displacement damage need to be considered
  - Size, weight, and power (SWaP) optimization

Questions? Thank you!

Contact information

Name	Role	Email	Phone
Esko Mikkola	PI	Esko.Mikkola@alphacoreinc.com	520-647-4445
Matt Engelman	Program Manager	Matt.Engelman@alphacoreinc.com	520-289-3897

Alphacore, Inc.
398 S. Mill Ave., Suite 304
Tempe, AZ 85281
www.alphacoreinc.com