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DOE-NP SBIR/STTR EXCHANGE MEETING

Radiation Tolerant SOI CMOS Detectors

DE-SC0002421 & DESC0004237 (topic 49d)

Dr. Manouchehr Farkhondeh

GEORGE M. WILLIAMS

VOXTEL INC.

"Detector funding in Europe is good; in Japan, modest; but in the US, totally inadequate."

Chris Damerell of Rutherford Appleton Laboratory and chair of the Detector Panel, SNOWMASS 2005

About Voxtel

Corporate Offices / Voxtel Opto (Beaverton, Oregon)

- **Contract Administration**
- **Opto Products Group**
  - **Detectors:** InGaAs and silicon photodiodes, avalanche photodiodes (APDs), photoreceivers, and focal plane arrays
  - **Integrated Circuits:** Readout integrated circuits (ROICs) for imaging, LADAR, and radiation detection
  - **Single-Photon and Time-Resolved Detectors and Instruments**
  - **Electro-Optic Systems Engineering**

Voxtel Nano (Eugene, Oregon)

- **Nano Products Group**
  - **Colloidal Semiconductor Quantum Dots (PbS, CdSe, InP, SnTe, CIS, CZIS, etc.)**
  - **Rare-earth-doped Nanoparticles (ZnS, YVO_4, LaF_3, etc.)**
  - **Ligand Design and Custom Surface Functionalization**
  - **Up- and Down-Conversion Optical Devices**
  - **Security Inks and Covert Taggants**
  - **Nanocrystal-sensitized Detectors and Solar Cells**
  - **Continuous Flow Reactor Nano-factories**
- **Analytical Facilities**
  - **SEM, HRTEM, VIS-NIR, PL, UPS/XPS, TGA, etc**

The Problem Facing Functional Silicon Detector Developers

Detector Requirements	Sub-micron CMOS
1. Analog/ Mixed signal	1. Digital
2. High resistivity (4 kΩ/cm)	2. Low resistivity (5 Ω/cm)
3. Thick electrically/optically active layer	3. Thin electrically active layer
4. High biases (5 VDC → 50+ VDC)	4. Low voltage (0.9– 1.8 VDC)
5. Thick, thermal oxides with ultra-low leakage	5. Thin high k+ oxides
6. Large, high linearity capacitors	6. Standard process flows
7. Full wafer integration	7. Full reticle integration (22 x 22 mm^2)
8. Custom materials, process flows and implants	8. No variability in materials or process
9. < 5" wafers available from R&D & MEMS fabs	9. 300 mm (+) wafers
10. Trained domestic work force	10. Trained work force

Today's CMOS processes are increasingly antithetical to high performance detector processing, and high-volume detector manufacturing capacity in the US is rapidly decreasing

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Potential Opportunities for Detector Developers

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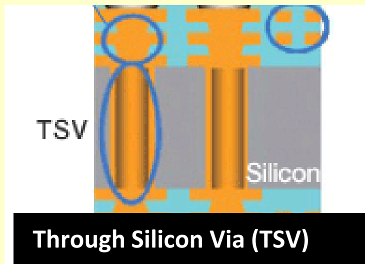
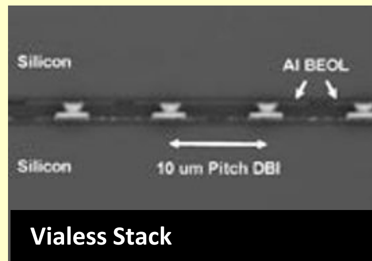
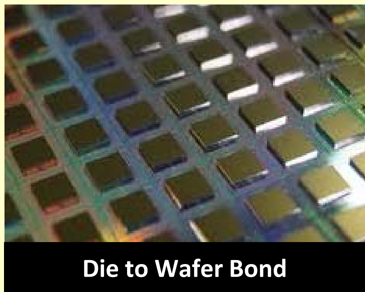
Via-less and TSV 3D Wafer Stacking

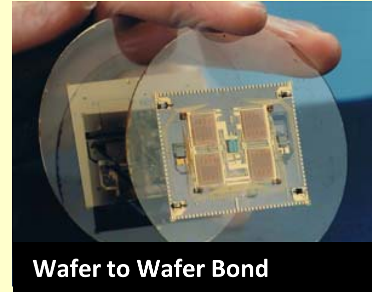


Through Silicon Via (TSV)

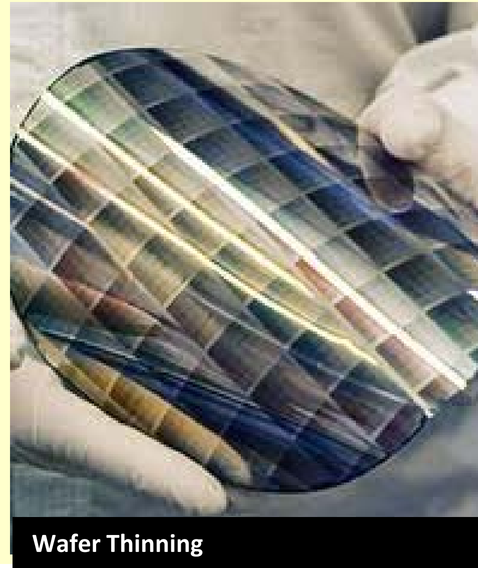


Vialess Stack

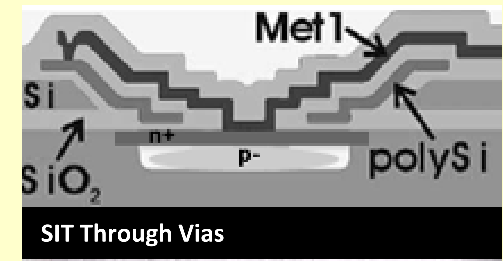

Die to Wafer Bond


Wafer to Wafer Bond

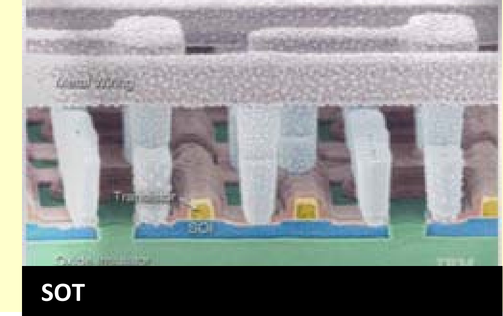
Wafer Thinning


Wafer Thinning

Through BOX SOI Wafers



SIT Through Vias


SOT

Exciting Advances Continue To Drive CMOS Advances. *<u>However,</u>*

- **Back-end of Line (BEOL) processes largely inaccessible to detector developers**
  - developed on 200+ mm wafer tooling (not widely available for custom development)
  - require full wafers, not multi-project chips (0.18 µm reticle costs w/first lot is ~$480K)
  - when wafer stacking is used, twice the cost (2x $400K / 0.18 um masks)
- **No sources of SOI CMOS through-BOX Vias**

Detector Solutions Available

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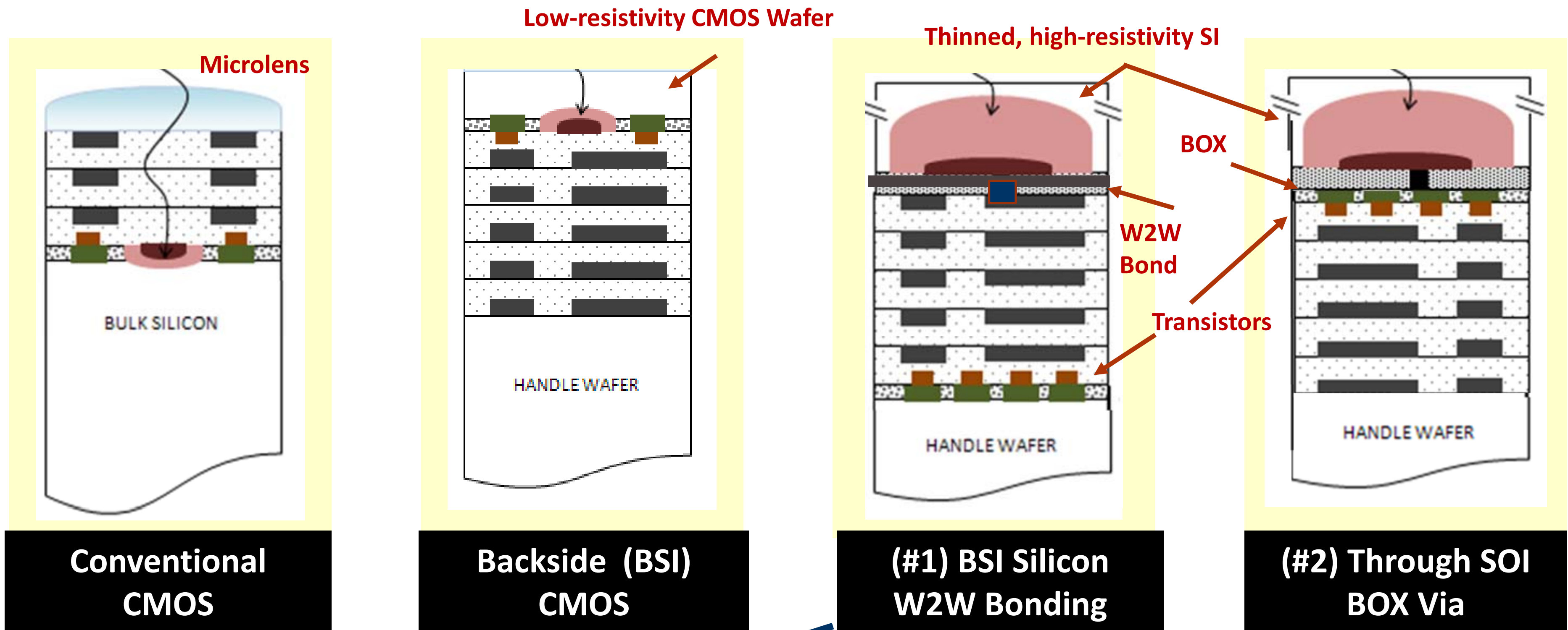

APPROACH #1

Stacked ROIC Circuit/Detector Layers

- High resistivity Si (Ge) detector layer
- W2W allows thick Si layers
- TSV - reduces fill factor
  - only good for thin Si

APPROACH #2

Monolithic with Detector in SOI Wafer

- Use SOI Substrate with low-rho top layer and high-rho bottom layer
- Requires through BOX via
- Self-aligned process, no 1um wafer alignment

Domestic (Hybrid) SOI-CMOS Process

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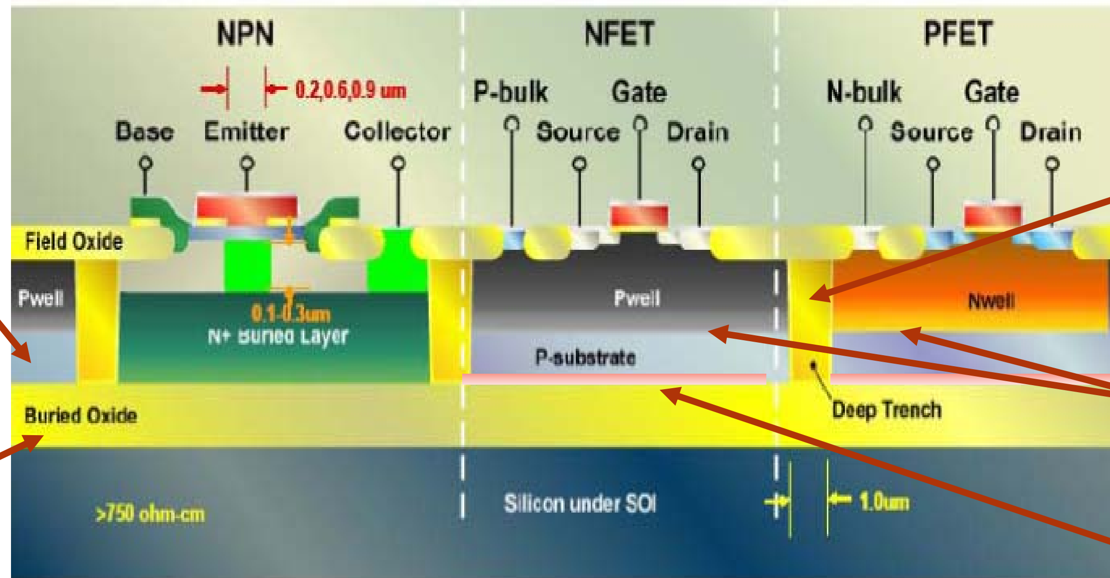
Bulk Si Islands can be used for detection

BOX minimizes SET and increases radiation tolerance



Trench Isolation Provides Electrical/Optical Isolation

Both Pwell and Nwell transistors available for circuits

P+ implant useful as substrate contact

Jazz/Tower Semiconductor CA18HJ Process

- bulk transistors fabricated on SOI wafers
- transistors isolated from one another with trench isolation (TI)
- SOI device layer is thick enough (1.4 µm) to prevent ‘back-gating’ of transistors and thin enough to minimize radiation-induced ionizing charge.
- buried implant between the BOX and the transistor layer prevents ‘back-gating’
- BOX is a good etch stop for back-thinning
- *however, 1.4 um not thick enough for many applications*

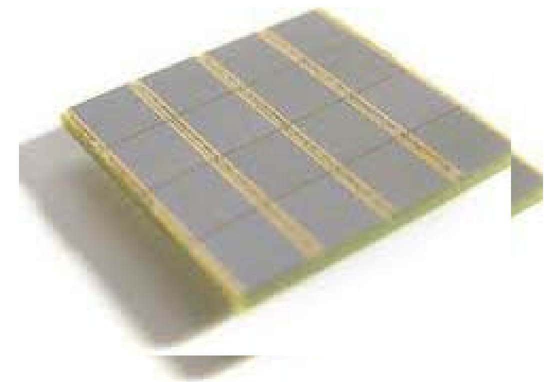
DOE 06157:

UV-Blue Enhanced Silicon Photomultipliers for Scintillators

Problem

Silicon Photomultipliers (SiPMs) have been proposed as photomultiplier tubes (PMTs) replacement for NP and medical application, *but*

- low detection efficiency and fill factor
- high, variable (inter and intra device) dark count rates
- not sensitive to scintillator output
- too expensive
- fabricated on old generation CMOS (now R&D) fabs
- large resistance/capacitance, which limit timing
- external ADC and functional circuits



Solution

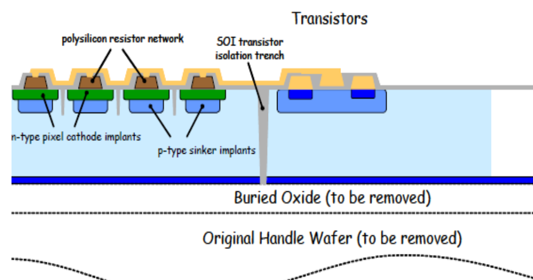
Digital SPADs made using SOI

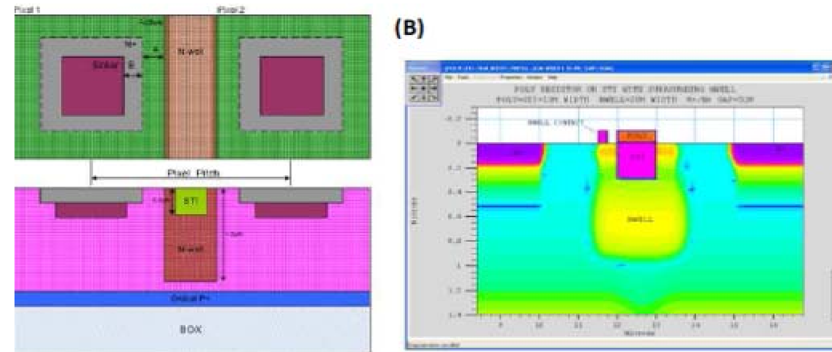
1. thin SOI layer for UV-VIS (particle?) detection
2. trench isolation electrically/optically isolated micro-cells
3. isolated SOI transistors used to increase detector functionality
   - bit enable, active quenching, uniformity correction, timing, counting
4. radiation tolerant

VOXTEL OPTO

Improved Silicon Photomultiplier Technology: SOI CMOS Digital Single Photon APD (DSPAD)

VOXTEL OPTO



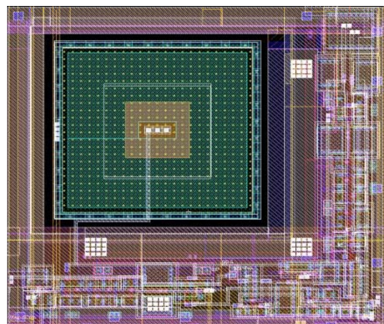


SOI Layer used for detectors

- SOI BOX layer used for thinning
- Buried p+ implant for substrate contact

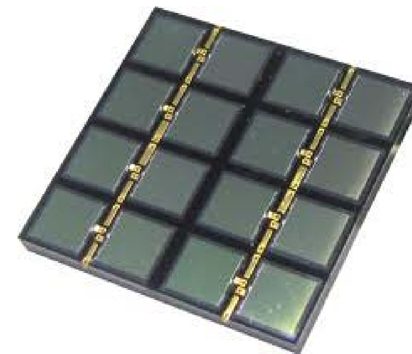
Geiger Mode (Gm) Si APDs formed in SOI layer

- Deep trench isolation (DTI) avoids optical cross-talk
- Layer fully depleted for fast response



Each SPAD microcell includes:

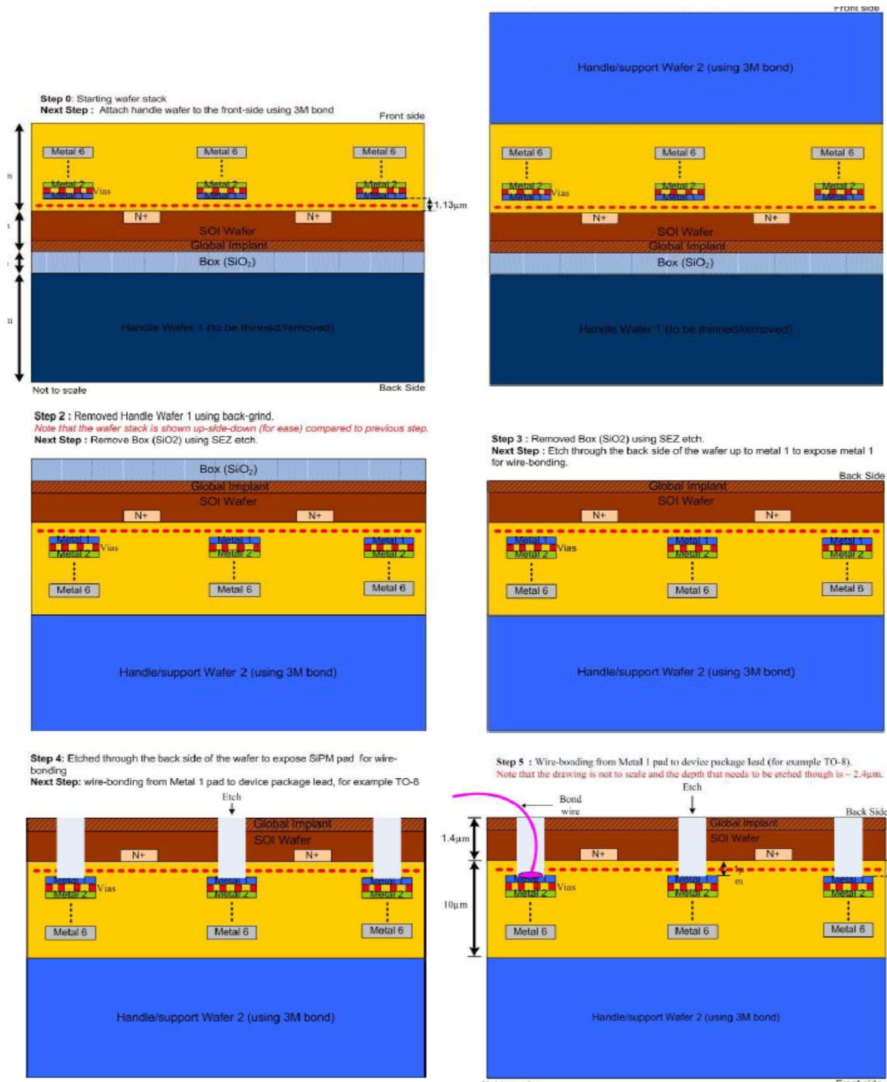
- Cell enable/disable
- Active quenching
- Programmable pulse comparator and holdoff
- 4-bit APD bias non-uniformity



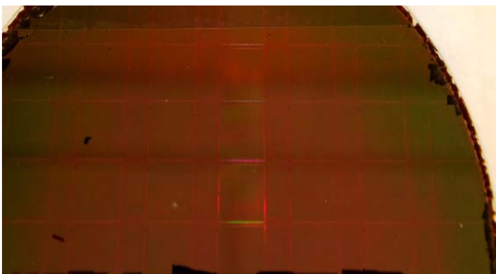
Each Pixel Includes

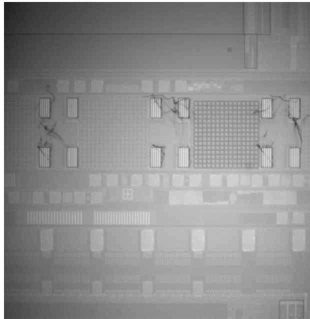
- Digital Counter (16-bit) and 200-ps time stamp in each pixel

Back-thinning SOI Wafers



Back-thinning of wafers





Back-thinned DSPAD Wafers

Semiconductor Tracking Detectors

DOE NP SBIR Contract # DE-SC0002421

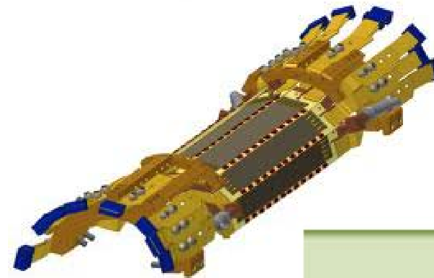
Statement of Problem

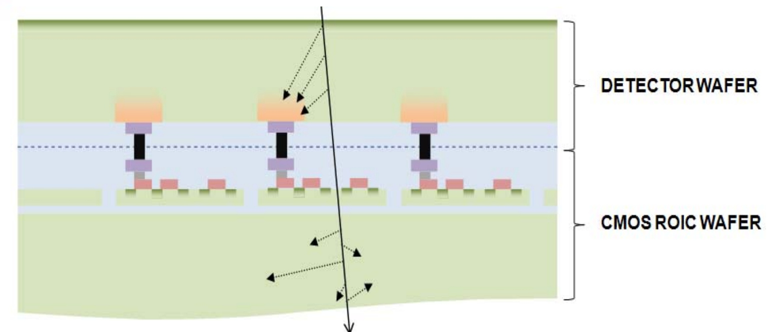
Existing CCD Trackers are:

- too slow,
- too expensive,
- too thick,
- data bandwidth intensive.

and CMOS imagers are:

- lack sensitivity,
- small detective cross section,
- not rad hard.





Approach

- **3D Wafer stacking of detector layers to CMOS**
- **Small pixel / thin silicon for resolution/occupancy**
- **Record time –of-flight (tof) and amplitude**
- **Use sparsified data readout**
- **Use stitching to photo-compose large imagers**
- **Enclosed transistors w/SOI for radiation tolerance**

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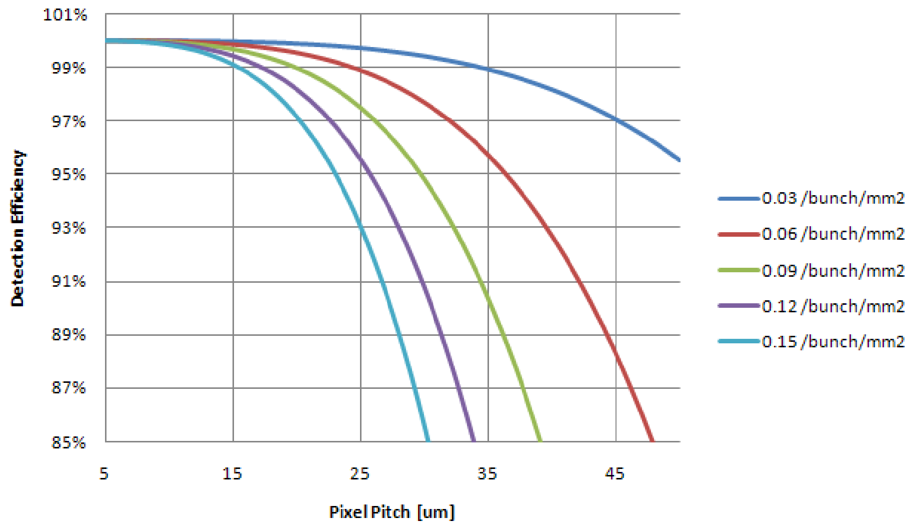
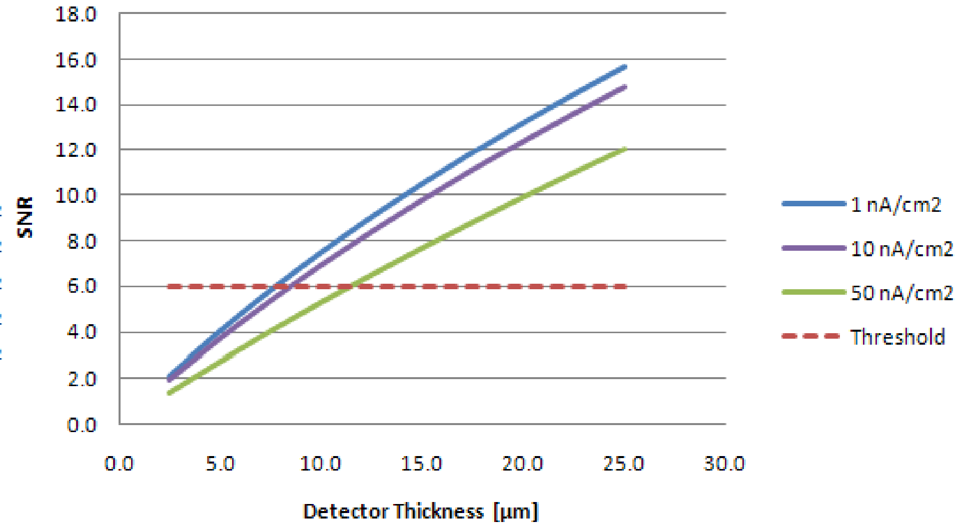
Specifying Tracking Focal Plane

VOXTEL OPTO



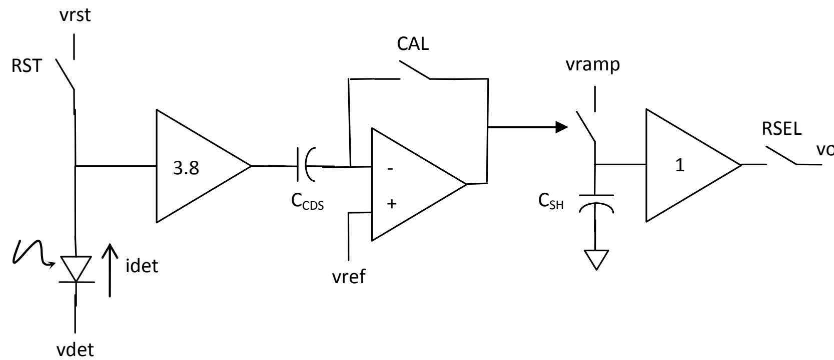
Detection efficiency analysis, assuming single event storage per pixel.



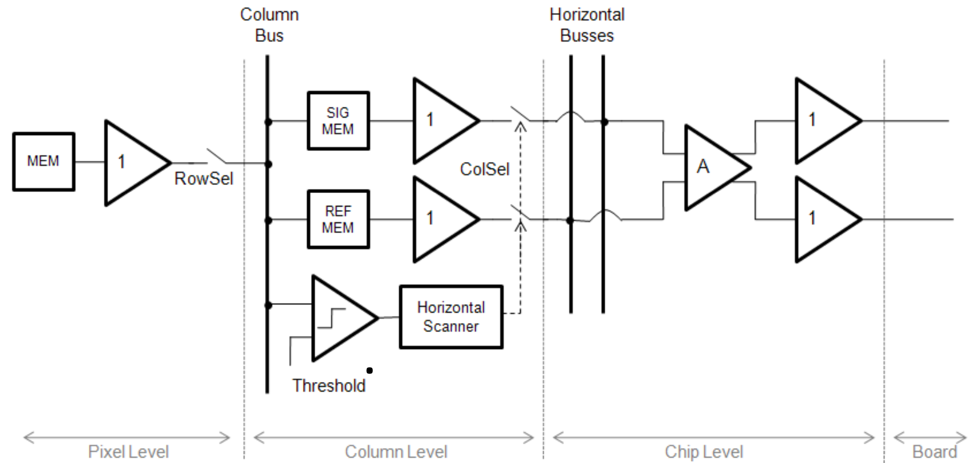
STN calculated as a function of detector thickness (read noise: 22 e−, pixel pitch: 15 µm; integration: 1 ms)

- **Pixel sizes of 15 µm have detections efficiencies larger than 99%, even with occupancies in excess of 0.15 events/bunch/mm²**
- **About 12-um thick detector WITH LOW AMPLIFIER NOISE achieves sufficient STN**
  - **– thin silicon minimizes dark current**
  - **- thin detectors tightens detector ring diameter**
  - **- small pixels with thin detector layer reduces multiple pixel events**

Tracking Detector Circuits

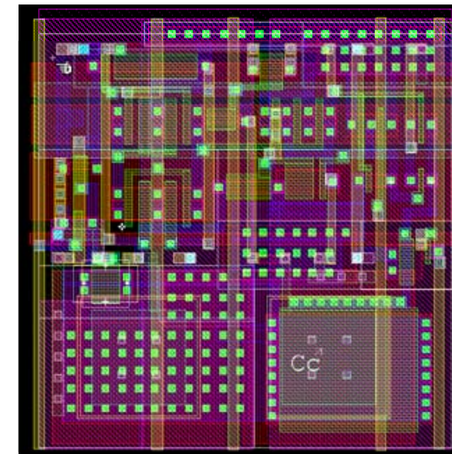


Vertex Detector: Pixel Block Diagram



Vertex Detector: Sparse Readout Architecture

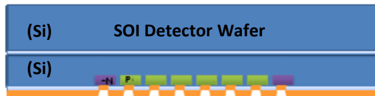
- Each pixel uses direct integration followed by an auto-calibrated comparator.
- Output of comparator samples the event ramp signal
- Time-of-arrival and amplitude data read out between frames.
- Readout uses pixel-, column-, and chip-level CDS to reduce fixed-pattern noise sources on the ROIC.
- Sparse scanning and pixel readout,
  - column read out if column flag indicated pixel "hit"

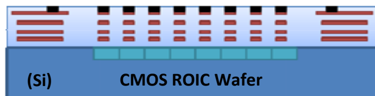


Vertex Detector: 15 µm Pixel

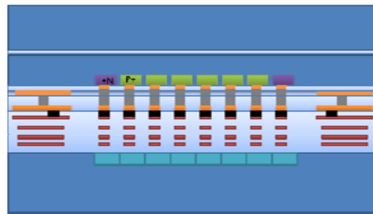
- in-pixel comparator is 70% of the pixel area

Via-less Wafer-to-Wafer Bonding



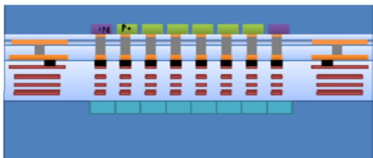


Starting Materials: SOI detector wafer has global Al deposition; CMOS ROIC wafer is planar with last VIA up to surface.



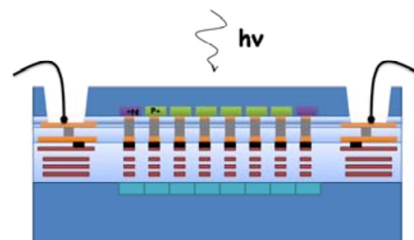
Step 5: Bond SOI detector and ROIC wafers at room temperature following preparation with NH_4OH solution.

Step 1: CMOS ROIC wafer receives a global seed metal (Al) deposition. SOI detector wafer already has global seed metal.



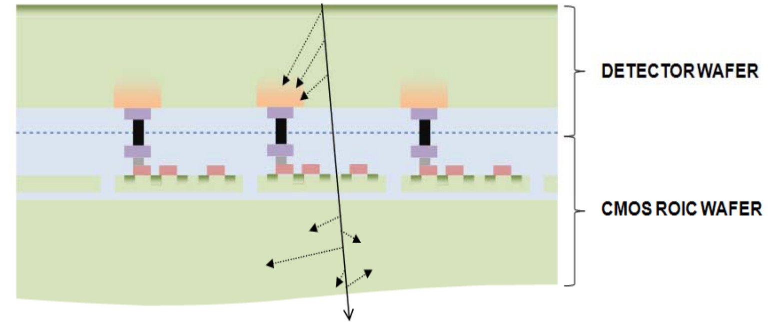
Steps 6-7: Grind away silicon handle wafer of SOI within 50-µm of BOX. Remove remaining Si handle and BOX using wet etch process.

Steps 2-4: Both wafers pattern/plate DBI metal (Ni), etch seed metal, and receive oxide deposition/planarization.



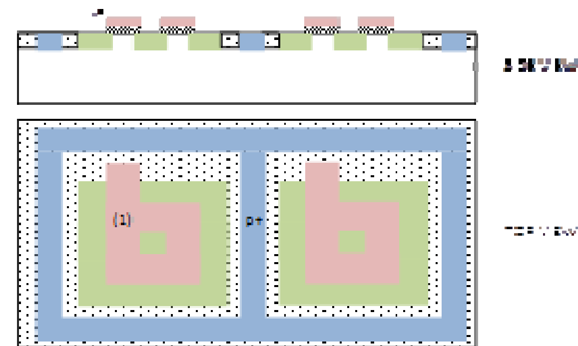
Steps 8-9: Remove Si material above CMOS ROIC bond pads. Open SiO_2 passivation above ROIC pads. Package device.

Wafer-to-wafer Bonding Process



Bonded Detector

- Standard SOI CMOS ROIC wafer (bottom),
- High-resistivity silicon detector (top)
- Wafers bonded using direct-oxide bond
- <15-µm pitch; < 20-um total thickness .



Enclosed-layout transistors (ELTs).

- Leakage paths are removed using the enclosed layout with p+ guard rings,
- Radiation tolerant

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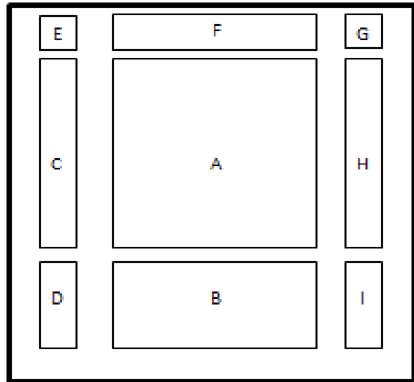
Photocomposition of Large Areas via Stitching



Reticle Block Layout (22 mm x 22 mm)
Block A: Pixel array (1024 x 1024)
Block B: Analog readout / Horz. scanner
Block C: Vertical scanner
Block D: Digital control
Block E: Top left pixel array corner
Block F: Top pixel bussing
Block G: Top right pixel array corner
Block H: Right pixel bussing
Block I: Global biasing

E	F	F	F	F	F	F	F	F	G
C	A	A	A	A	A	A	A	8k x 8k A	H
C	A	A	A	A	A	A	A	A	H
C	A	A	A	A	A	A	A	A	H
C	A	A	A	A	A	A	A	A	H
C	A	A	A	4k x 4k A	A	A	A	A	H
C	A	A	3k x 3k A	A	A	A	A	A	H
C	A	A	A	A	A	A	A	A	H
C	A	A	A	A	A	A	A	A	H
D	B	B	B	B	B	B	B	B	I

Layout of Reticle

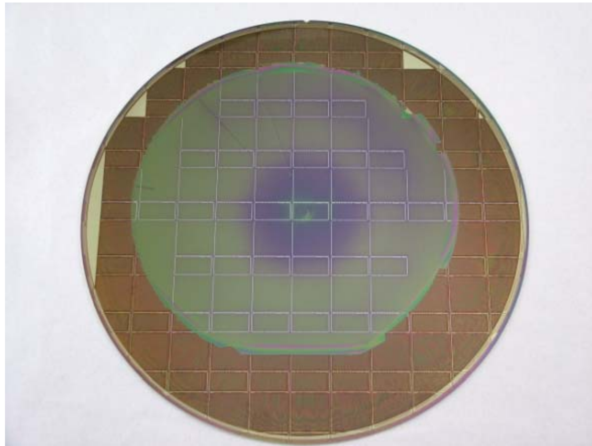
Photocomposition of Large Arrays is used for Fill Wafer Integration.

CMOS Reticles are only about 22 x 20 mm^2, so larger detector areas must be decomposed into structural components and photocomposed

- allows design to be redeployed for various applications without $500K mask investment

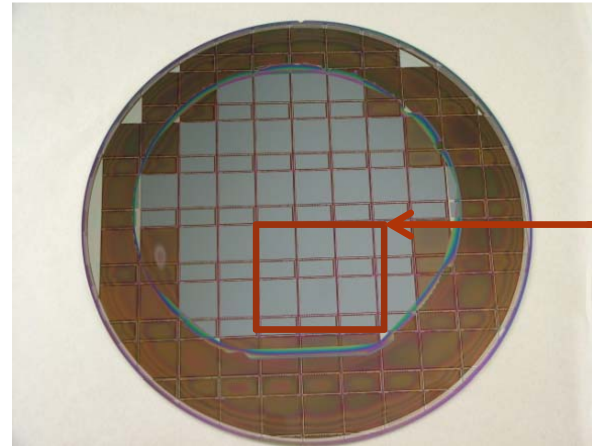
Backthinning Bonded Wafers

VOXTEL OPTO



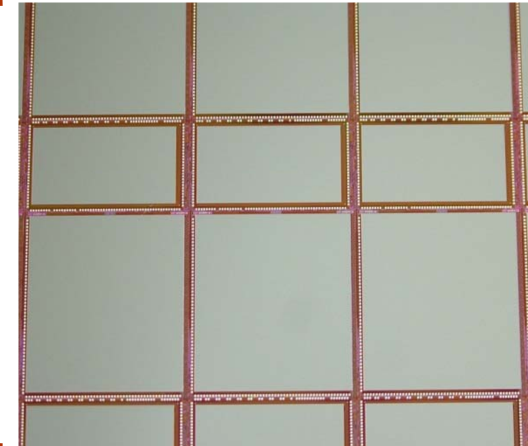
Bonded VX-802 wafer before thinning

- 200-mm ROIC wafer bonded to 150-mm detector wafer
- Detector layer 20 um thick



Bonded wafers
After thinning

- detector mesas formed and bond pad openings etched



Zoom of device (large square) in wafer form.

- gray areas are detector mesas small pads in brown areas are the bond pads.

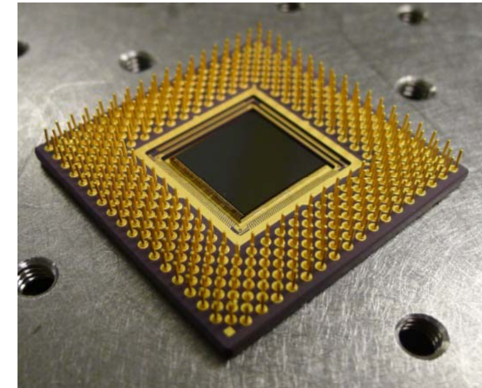
- **Wafer bonding with face-to-face Via-less interconnection (Ziptronix)**
- **150mm high resistivity silicon detector wafer**
  - **- Surface functionalized with bond metal and oxide treatments**
- **SOI Detector layers thinned (down to BOX layer) to reveal detectors**
  - **- Device bonded to backside of pads revealed after etch**

VX-802 Performance Specification

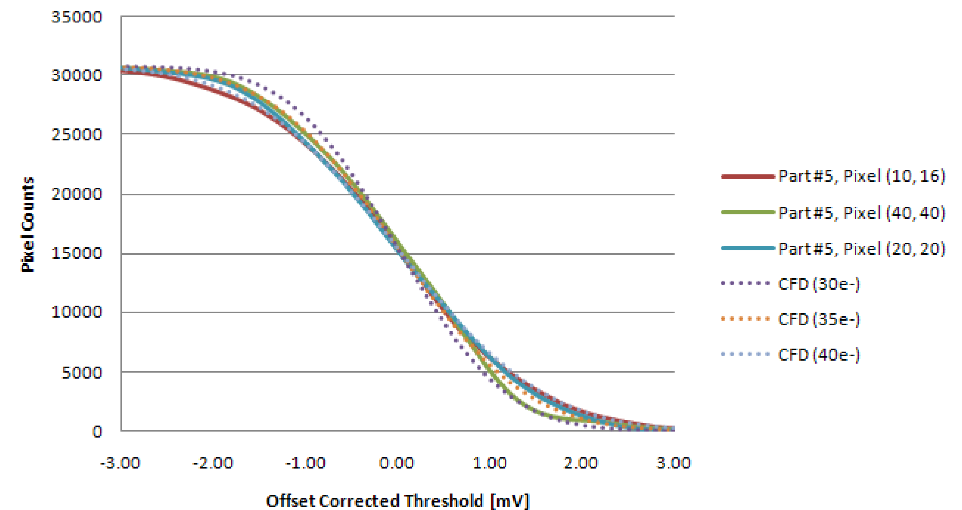
VOXTELOPTO

Resolution	pixels	960 x 448
Detector Area	mm	16 x 7.5
Butability	-	-
Pixel Pitch	µm	15.0
Detector Thickness	µm	20.0
Detector Capacitance	fF	1.2
Dark Current Density	nA/cm^2	3.5
Dark Current	fA	7.9
Detector Polarity	-	P-on-N
Event Rate	$/bunch/mm^2$	3.00E-02
Max Bunch Rate	ns	337.0
Bunches per Train	bunches	2820
Frame Dead Time	ms	199
Particle Charge	e-	1000.0
Integration Time	ms	1.0
Pixel Noise	e- RMS	20.0
Threshold Dispersion	e- RMS	< 5.0
Timing Dynamic Range	bits	11.5
Timing Resolution	ns RMS	350
Event Depth	-	1
Conversion Gain	µV/e-	70.3
Total Noise	e- RMS	38.1
Signal Noise Ratio	-	26.3
Power Consumption	mW	80.0
Readout Scheme	-	ITR - sparse or full
Radiation Tolerance	krad	20

Specification



VX-802 design packaged in ceramic PGA.



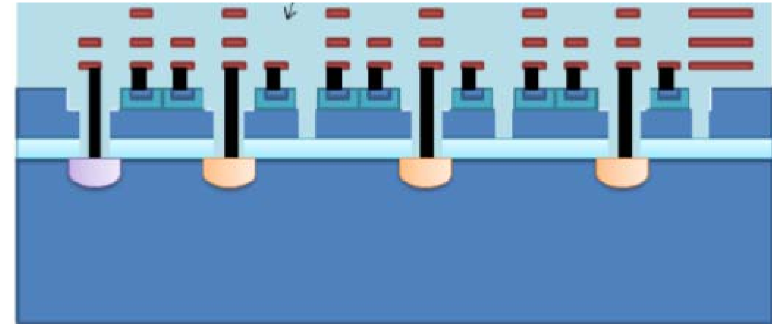
Measurement of pixel detection events in slow mode (low bandwidth)

Commercial CMOS Foundry for Particle Detectors

DOE Contract # DESC0004237 /SBIR Topic: DOE NP 44d

Statement of problem

- **Existing hybridized detectors have penalizing noise, granularity, and thickness due to**
  - **due to thin CMOS APS depletion**
  - **sharing of process with detection implants**
  - **integration techniques (e.g. bump bonding)**
- **CMOS limited in size by 20 x 20 mm² reticle**
- **Large detectors expensive**



Monolithic SOI CMOS Detector: *Detector formed in high resistivity handle SOI CMOS wafer by implanting into handle and electrically interconnecting SOI circuits through vias in buried oxide (BOX)*

Approach

- **Develop a domestic foundry services of monolithic fully-depleted SOI CMOS imagers**
- **Key innovations include:**
  - SOI CMOS imager process
  - Custom engineered SOI wafers
  - Low dark current, low capacitance, silicon photodiodes fabricated in high resistivity silicon handle of SOI wafer
  - Low noise, radiation hardened ROIC design

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Monolithic SOI Pixel Detector Architecture

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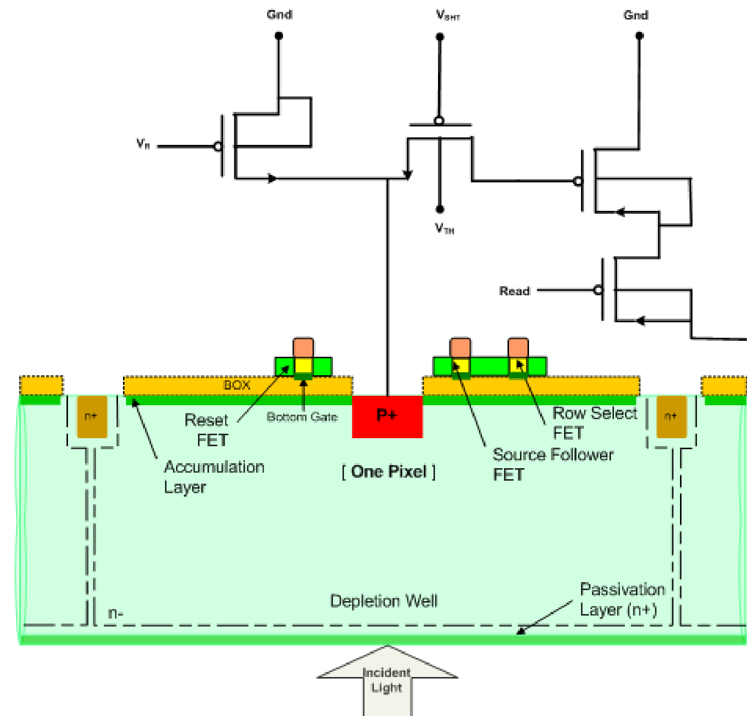
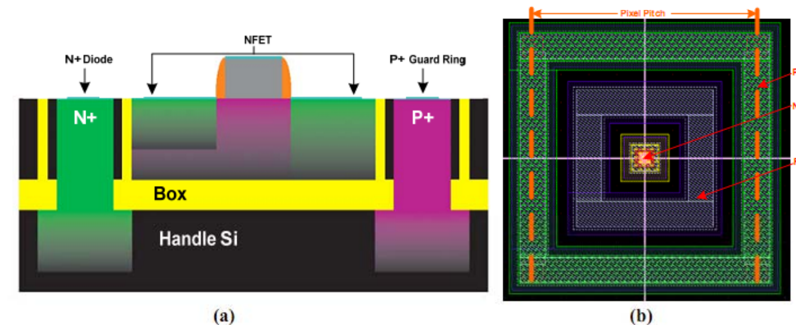
- Bonded double SOI (dSOI) wafer
  - high resistivity detector, low resistivity circuits
  - custom implants at each Si surface
- Standard SOI process
  - NMOS,PMOS, MIM caps, etc
- Isolated transistors
  - separate grounds for circuits and detectors
- Minimal Impact on CMOS Process
- Monolithic detector, with no bump bonds or 3D circuit stacking
- Can be very thin, fully-depleted
- High density (smaller pixel size is possible)
- Industry standard technology
  - cost benefit and scalability)





(a) (b)

SOI CMOS "Through BOX VIA" 3D Interconnect

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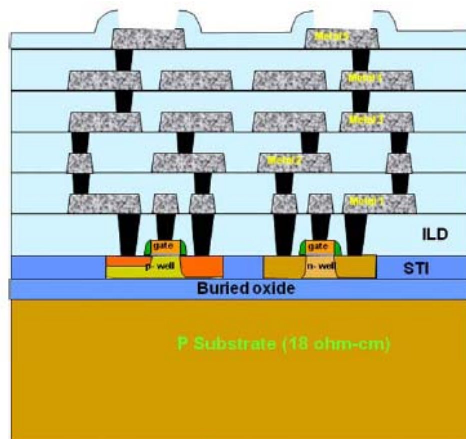
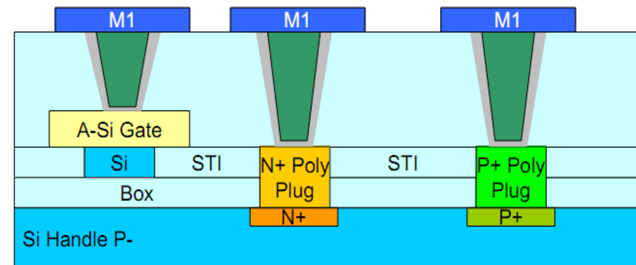
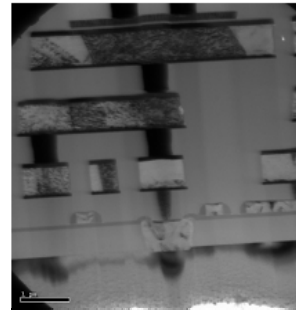


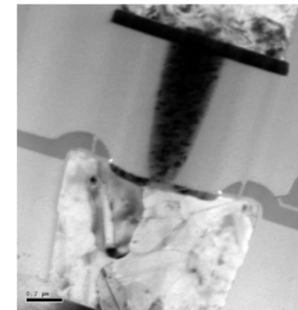
Sandia CMOS7 process:

- *5 metal distribution layers.*
- *MiM capacitors,*
- *n+ poly resistors, and*
- *0.35-μm feature length radiation hard FETs.*



Diode diffusions (p+ & n+) in handle wafer and doped polysilicon plugs through the STI for electrical interconnection


(a)


(b)

TEM of portion of Sandia pixel manufactured using poly plug after STI option.

- **Process is being developed on Sandia CMOS7 process**
- **Implementing photodiode implants and electrical interconnect through BOX**
- **Use custom SOI wafers with high resistivity handle**

Through BOX Via Process

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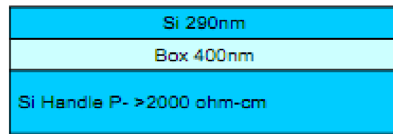
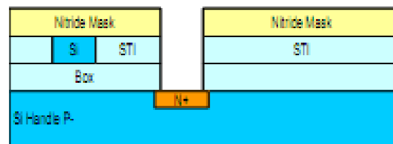
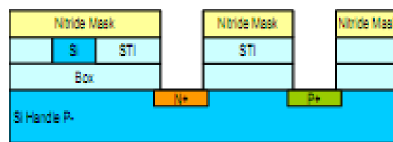
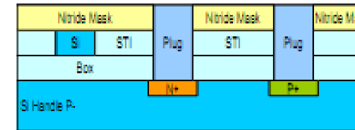
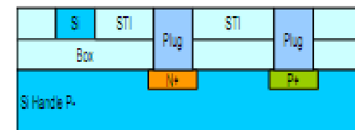
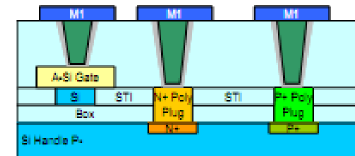


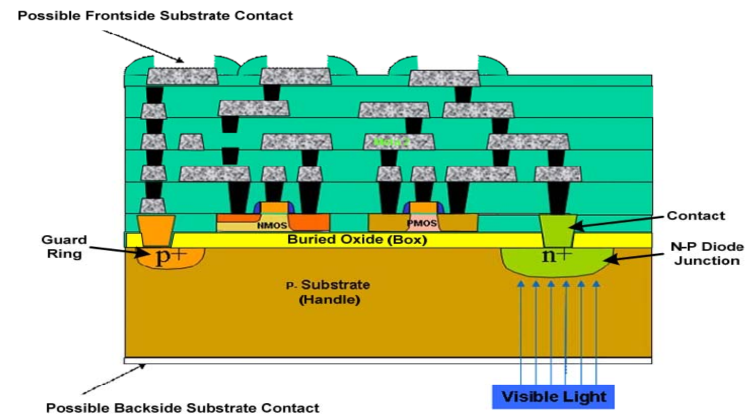






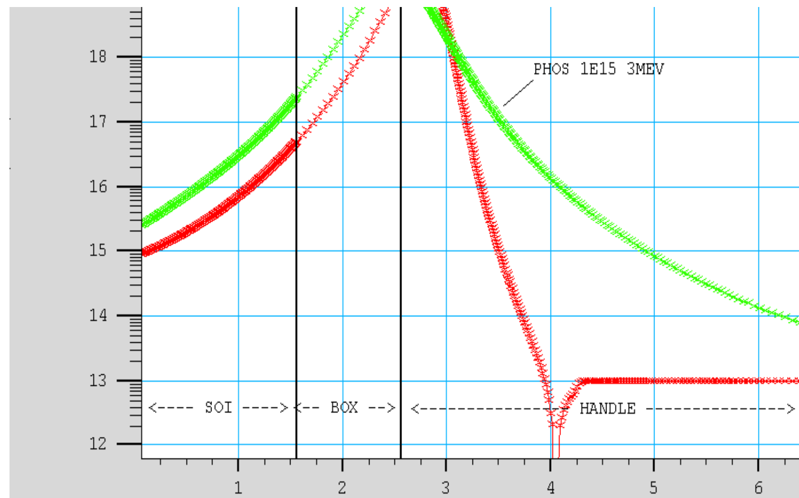




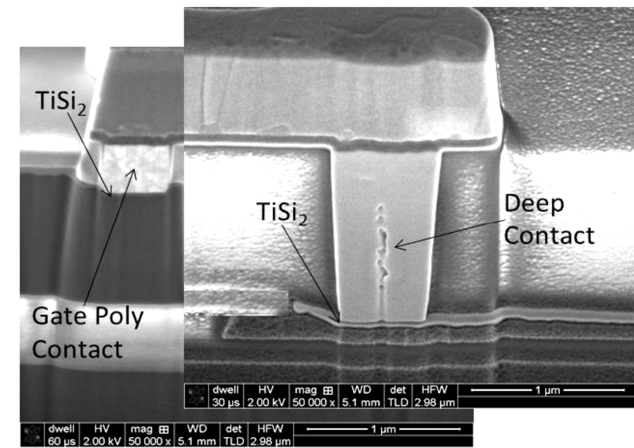


Implemented in SOI process

Results of Through BOX Process



Implants Used to Create Photodiode
- the high energy implants (> 1.5 MeV) must peak on bottom of BOX



FIB cross sections of deep contacts

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Prototype Array Currently Being Fabricated

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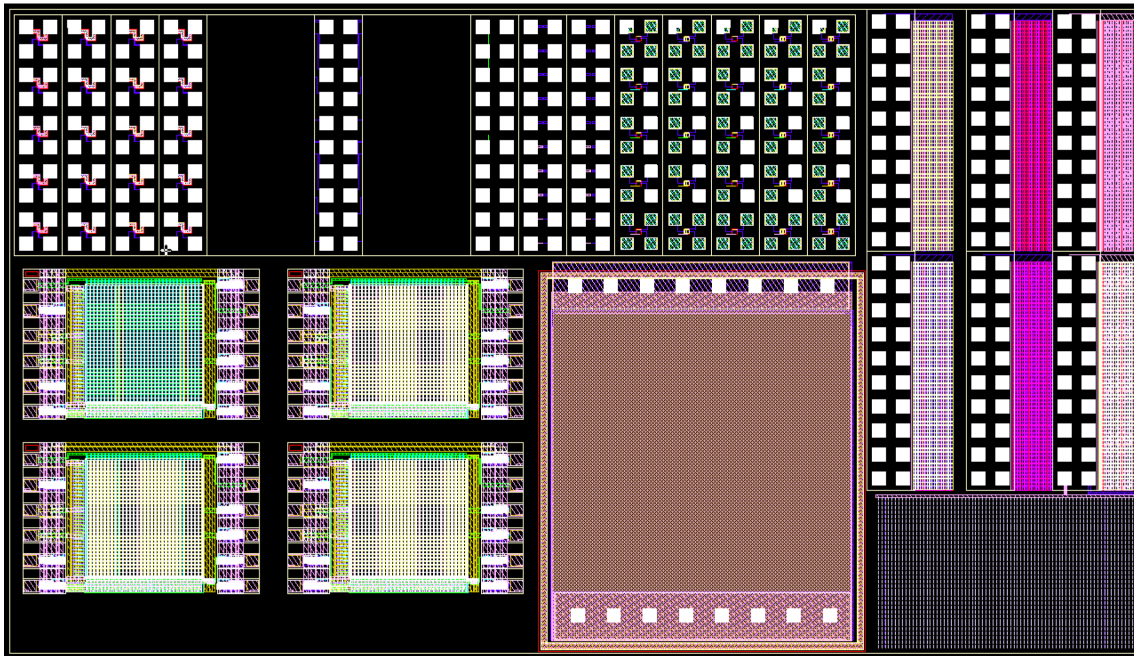
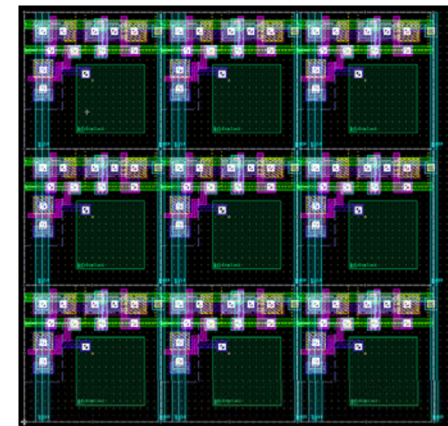


Layout of reticle being fabricated using through Si VIAs



SFD pixel shown in 3 x 3 array of pixels

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Thank You

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Voxtel Inc.
15985 NW Schendel Ave
Beaverton, OR 97006
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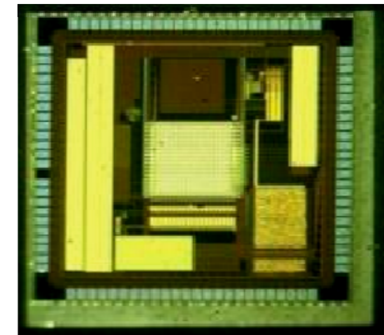
c. 503-703-3260

InGaAs Avalanche Photodiodes

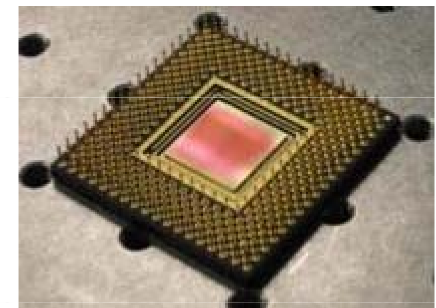


SiPM/DSPAD Arrays

Hermetic, TE-Cooled GHz-Class Receivers

Back-Illuminated, Microlensed InGaAs / InAlAs / InP FPAs

psec-Resolution Photon Counting Instruments



Large Format Sensors