Basic Research Needs for Microelectronics Workshop October 23-25, 2018:
Preliminary findings

Workshop Chair: Cherry Murray (Harvard Univ.)
Associate Chairs: Supratik Guha (ANL)
Dan Reed (Univ. of Utah)

Technology Liaison: Gil Herrera (SNL)
SC Technical Leads: Andy Schwartz (BES)
Robinson Pino (ASCR)
Eric Colby (HEP)

on behalf of DOE Office of Science
Basic Energy Sciences, Advanced Scientific Computing, High Energy Physics

Basic Research Needs ... Workshops

21 reports; 14 years; >2,000 participants from academia, industry, and DOE labs

- BRN to Assure a Secure Energy Future BESAC (2002)
- BRN for Hydrogen Economy (2003)
- BRN for Solar Energy Utilization (2005)
- BRN for Superconductivity (2006)
- BRN for Solid State Lighting (2006)
- BRN for Advanced Nuclear Energy Systems (2006)
- BRN for Geosciences (2007)
- BRN for Clean and Efficient Combustion (2007)
- BRN for Electrical Energy Storage (2007)
- BRN for Catalysis for Energy Applications (2007)
- BRN for Materials under Extreme Environments (2007)
- New Science for Sustainable Energy Future (2008)

- BRN for Carbon Capture (2010)
- Computational Materials Science and Chemistry (2010)
- Science for Energy Technology (2010)
- Controlling Subsurface Fractures and Fluid Flow (2015), Next Gen Tools(2016)
- BRN for Environmental Management, Energy-Water-Nexus (2016)
- BRN for Quantum Materials (2016)
- BRN for Synthesis Science (2016)
- BRN for Next Generation Electrical Energy Storage (2017)
- BRN for Future Nuclear Energy (2017)
- BRN for Catalysis Science to Transform Energy Technologies (2017)

- **BRN for Microelectronics (2018)**

http://science.energy.gov/bes/community-resources/reports/
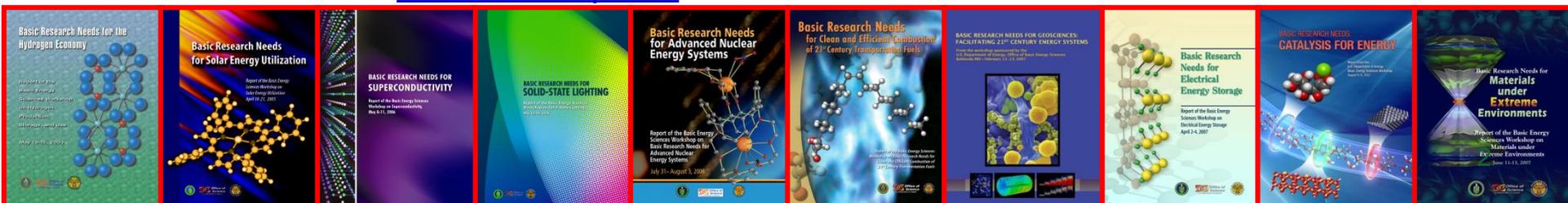
Basic Research Needs – Use Inspired Basic Research

- **Transformative, not incremental research directions**

- **Fundamental science challenges to move the technology forward**

- **New techniques and methods**

- **10-30 years out**

BRN for Microelectronics Workshop – Motivation

- Semiconductor-based microelectronics are critical to the U.S. economy, scientific advancement, and national security
  - Semiconductor products are currently the third largest class of U.S. exports (behind aircraft and automobiles)
  - U.S. companies account for more than 50% of the world market by revenue
  - Semiconductor industry directly employs ~250,000 people; ~1 million associated jobs
- The decades long success of Moore's Law was driven by innovation
  - Materials and chemical sciences
  - Computer science
  - Electrical engineering
  - Fabrication technologies
- Additional innovation needed to keep up with dramatic market growth

U.S. DEPARTMENT OF ENERGY | Office of Science

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Motivation: CMOS scaling slowdown

Logic transistors density (MTr/mm²) vs HVM Wafer Start Date

FINFET

HKMG

10nm — 2.7x
14nm — 2.5x
22nm — 2.1x
32nm — 2.3x
45nm

Intel

Intel Technol. & Manufacturer's Day, 2017
http://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2017/03/Mark-Bohr-2017-Moores-Law.pdf

Global Foundries

65nm 40nm 28nm 20nm 14nm FinFET

Transistor Cost / Technology Node
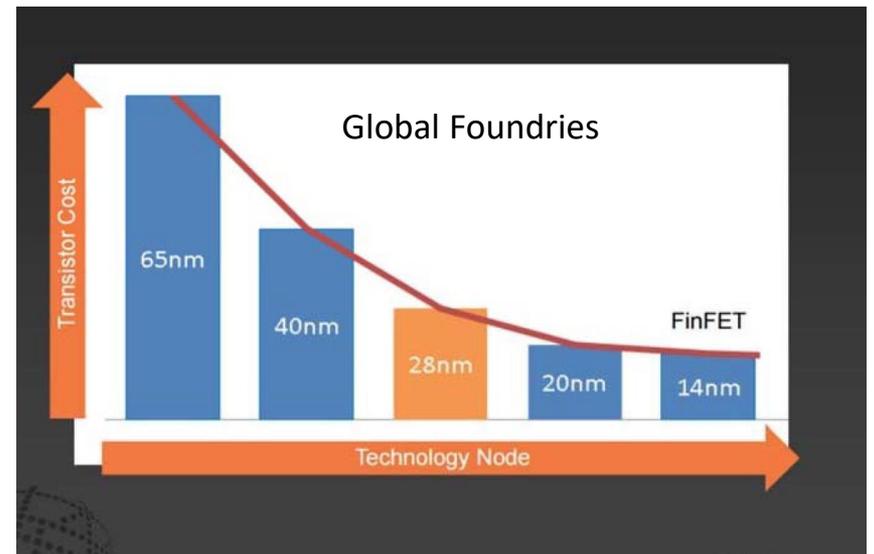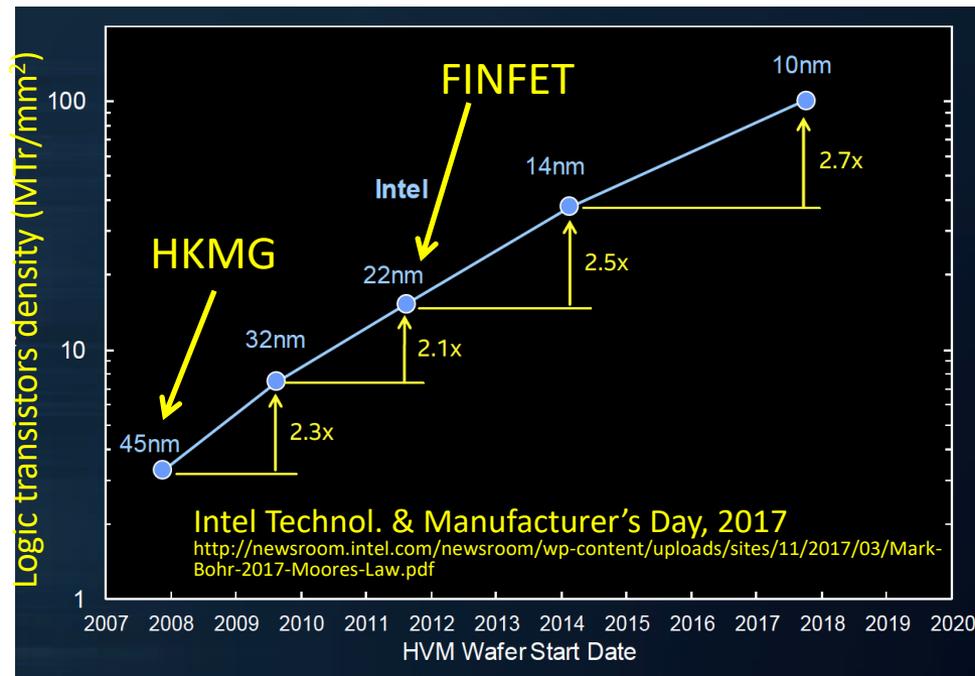
http://www.swtest.org/swtw_library/2015proc/PDF/SWTW2015_Keyr McCann_GlobalFoundries.pdf

Uncertainty at 7 nm node
complexity and cost
Physics gets in way

electrode
oxide
Source   Drain
silicon

bulk

Drain
Gate
Source
Oxide
Silicon Substrate

https://www.quora.com/What-is-a-FinFET-transistor
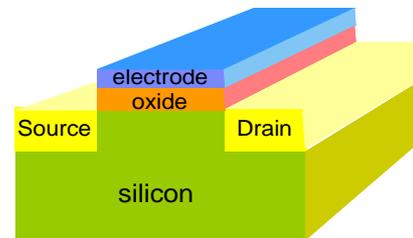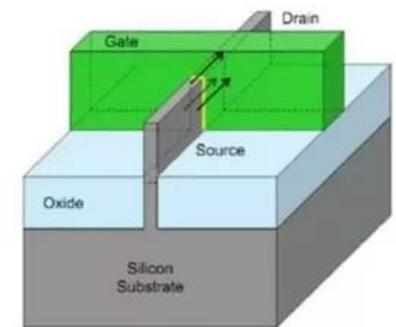
# Impact to computational materials science--example

Rise of data intensive & edge computing: future Compact Muon Solenoid (CMS) computing needs at Large Hadron Collider (LHC)

A data storage and movement problem

- Exa-byte scale disk and tape storage, 50x w.r.t. now

- CPU needs 5M cores, 20x w.r.t. now

- transfer of exa-byte-sized data samples across the Atlantic at 250-500 Gbps, (today: 40Gbps allocated by ES Net)
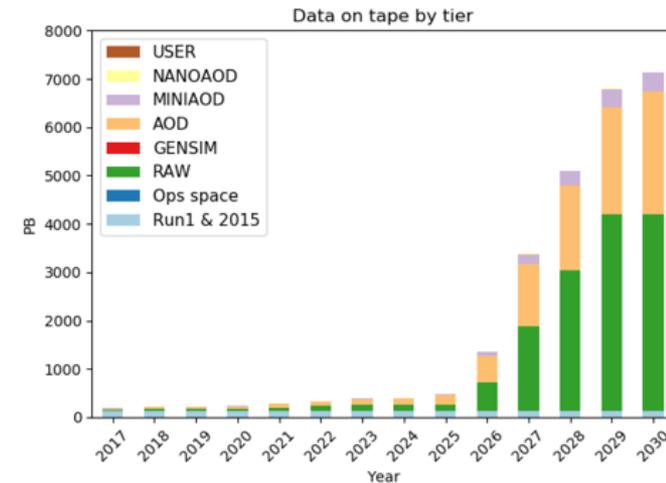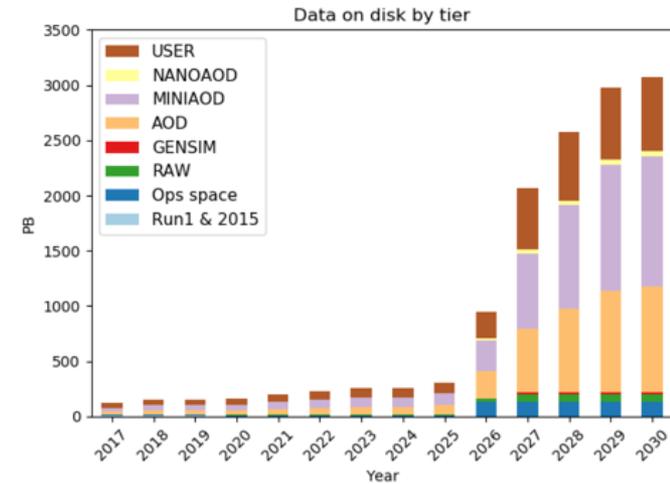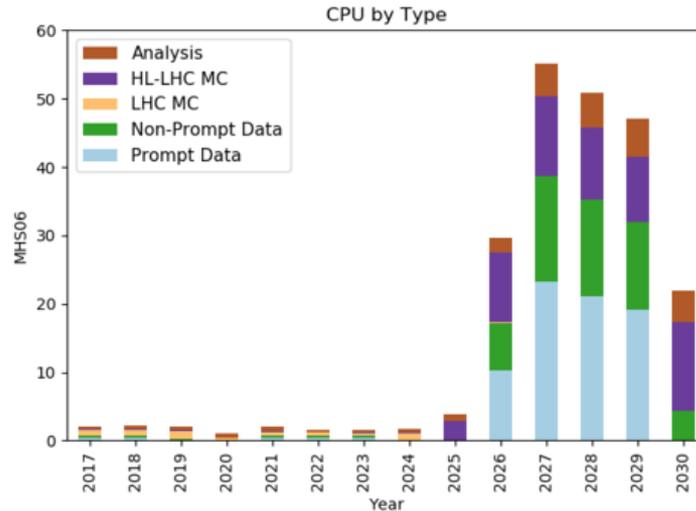
*(From talk by L Bauerdick, Fermilabs, conveyed by S. Habib, ANL)*

# Rise of data intensive & edge computing

Need for new computing paradigms

Memory bottlenecks
Data transport
Low power computing
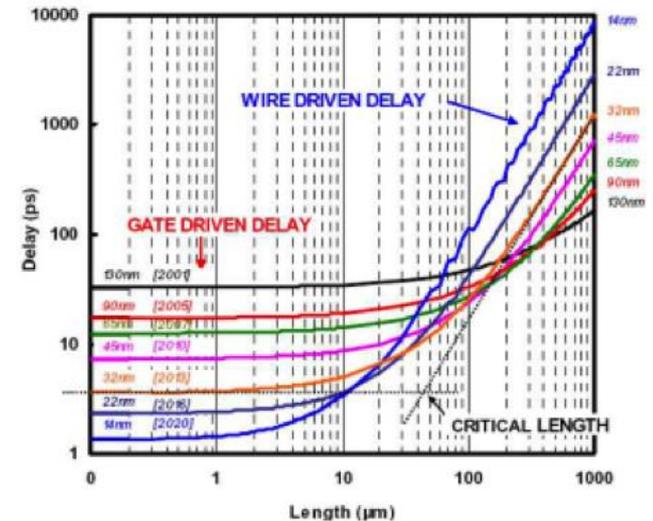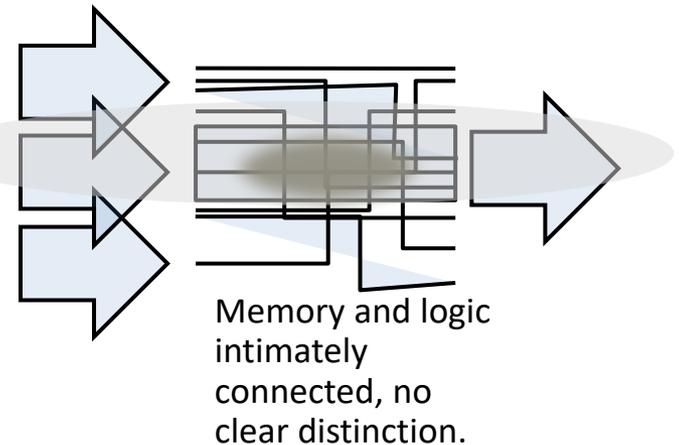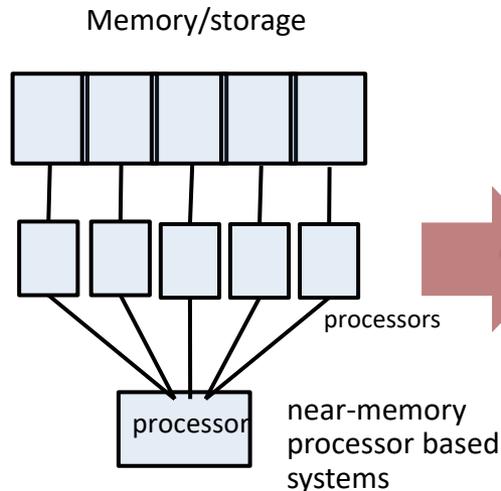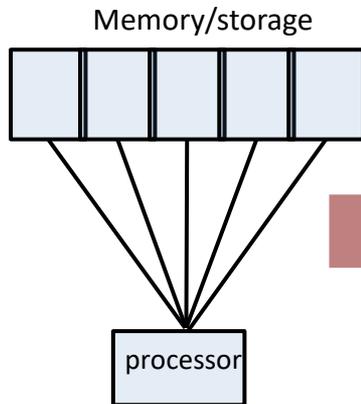

Source: M. Sellier, ISQED 2008

One approach

Memory/storage

Memory/storage

processor

processor

processors

near-memory
processor based
systems

Memory and logic
intimately
connected, no
clear distinction.

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Future Computing Technologies are Important to DOE
as well as many other Federal Agencies

- High-performance computing & simulation underpin DOE missions in energy, environment, and national security
  - Historical role of computing in DOE
  - DOE/vendor synergies in deploying computing technologies

- Future computing technologies (e.g., quantum, neuromorphic, probabilistic, etc.) hold promise for next-generation DOE mission applications
  - DOE research and facilities (e.g. HEP experiments, ASCR HPC, BES light sources) will depend on advanced computing and sensing technologies
  - Likely will augment, not replace, conventional supercomputing
  - Could open new avenues for use of computing in science (data analytics, machine learning, artificial intelligence, …)

- New directions for applied mathematics and computer science are likely to emerge that could enable new science across DOE-SC

Call To Action

- Significant challenges as CMOS extends below 5nm

- The end to Moore's Law will impact U.S. industry and competitiveness

- The importance of this issue and its technical complication will require *innovative approaches* to keep the U.S. in a leadership position

- Solving a problem of this scale will require *"whole of government"* approach and a robust *public/private partnership* to apply the best research from *industry, academia and government research facilities* to allow the U.S. to successfully make this technology transition

- DOE, and particularly the Office of Science, will play a significant role in this effort

- DOE-SC was charged with organizing a *Basic Research Needs Workshop* to define the highest priority research directions

Basic Research Needs for Microelectronics – Charge

- A thorough assessment of the scientific issues associated with advanced microelectronics technologies for applications relevant to the DOE mission.

- Identify critical scientific challenges, fundamental research opportunities, and priority research directions that require further study as a foundation for advances in microelectronics over the next decade and beyond.

- Particular emphasis on energy-relevant applications, and areas that are aligned with the missions and needs of ASCR, BES, HEP including data management and processing, power electronics, and high performance computing.

- Examine extension of CMOS and beyond CMOS technologies, **beyond exascale technologies. however Quantum Information Science is outside the scope of this workshop**.

- focus on a co-design innovation ecosystem in which materials, chemistries, devices, systems, architectures, and algorithms are researched and developed in a closely integrated fashion.

Innovation Opportunity Space

- Materials Research

- Device Physics

- Design and Fabrication

- Computer Engineering: architectures and micro-architectures

- Computer Science & Applied Math


- Other Considerations

  - *Outside the box*: Alternative materials, devices, fabrication techniques and architectures are likely to result

  - *Use-inspired science*: Function and application need to be considered at early stages

Basic Research Needs for Microelectronics Workshop participation

77 panelists, ~70 observers

By affiliation

- DOE Labs 39%
- Academia 39%
- Industry 18%
- Other Fed Agencies 4%
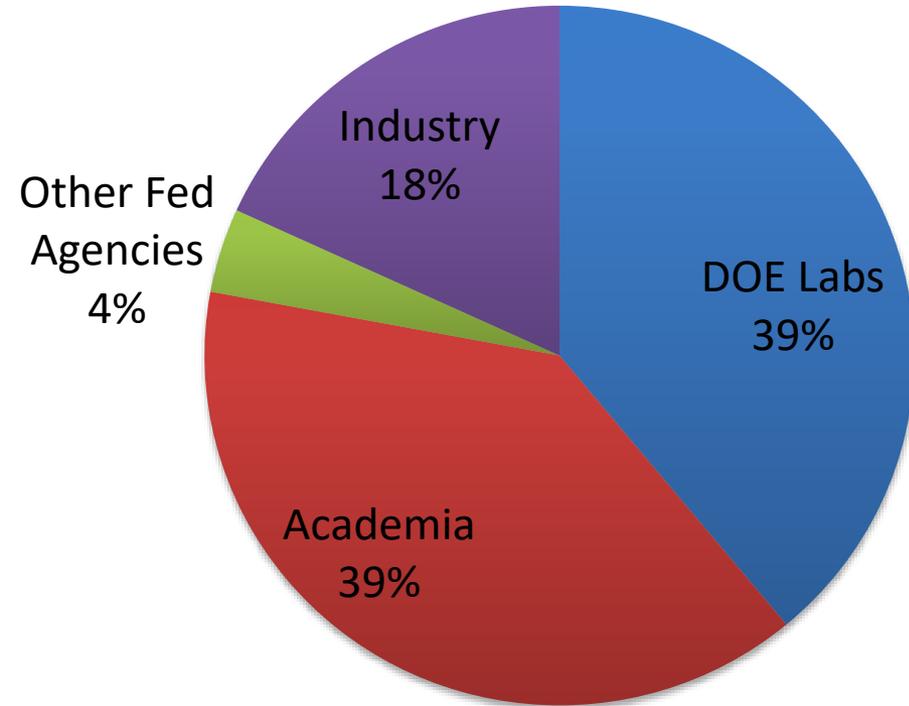
By expertise
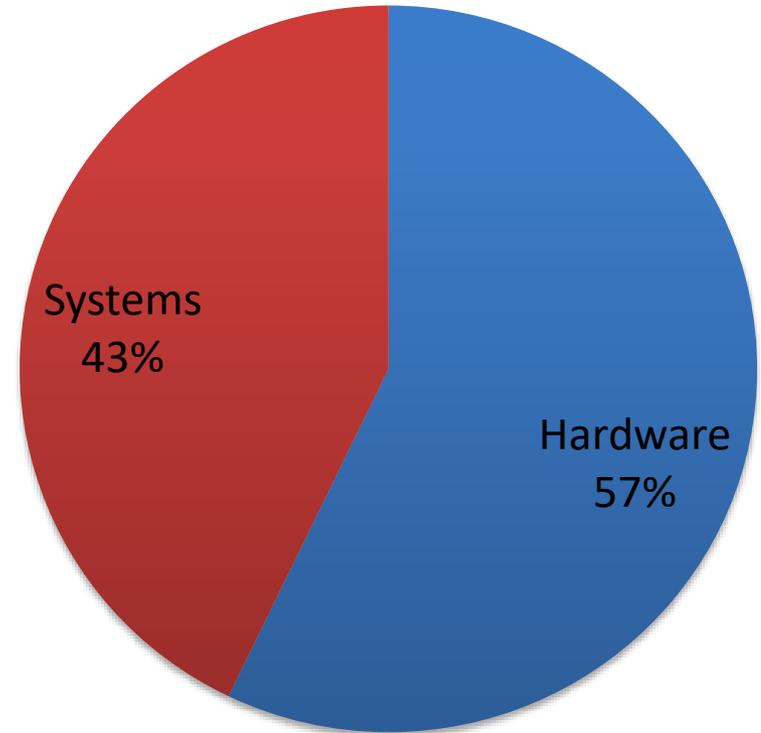
- Hardware 57%
- Systems 43%

<u>Systems</u>: circuits, micro-architecture, architecture, algorithms, software
<u>Hardware</u>: devices, materials, physics, chemistry

PLENARY TALKS TO SET THE SCENE AND PRESENT CHALLENGES

- **Justin Rattner (Intel, ret)**
- **Mike Witherell (LBNL)**
- **Bill Chappell (DARPA)**
- **Tsu-Jae King Liu (UC Berkeley)**
- **Dushan Boroyevich (VA Tech)**

Panels

Panelists were invited for their expertise – and are assigned to a particular panel that will determine priority research directions in the breakout sessions

1) Big data collection, analytics, processing for SC facilities
Leads: Kirsten Kleese van Dam (BNL) and Sayeef Salahuddin (UC Berkeley)

2) Co-design for high performance computing beyond exascale
Leads: James Ang (PNNL) and Thomas Conte (Georgia Tech)

3) Power control, conversion and detection
Leads: Debdeep Jena (Cornell U) and Robert Kaplar (SNL)

4) Crosscutting themes *– may roam and join other panels*
Leads: Harry Atwater (Caltech) and Rick Stevens (ANL)

Oct 22-25

Panel discussions → Themes .... → First cut PRDs .... → 2nd round panel discussions → Revised PRDs ....

Co-chairs+DOE team

Co-chairs+DOE team
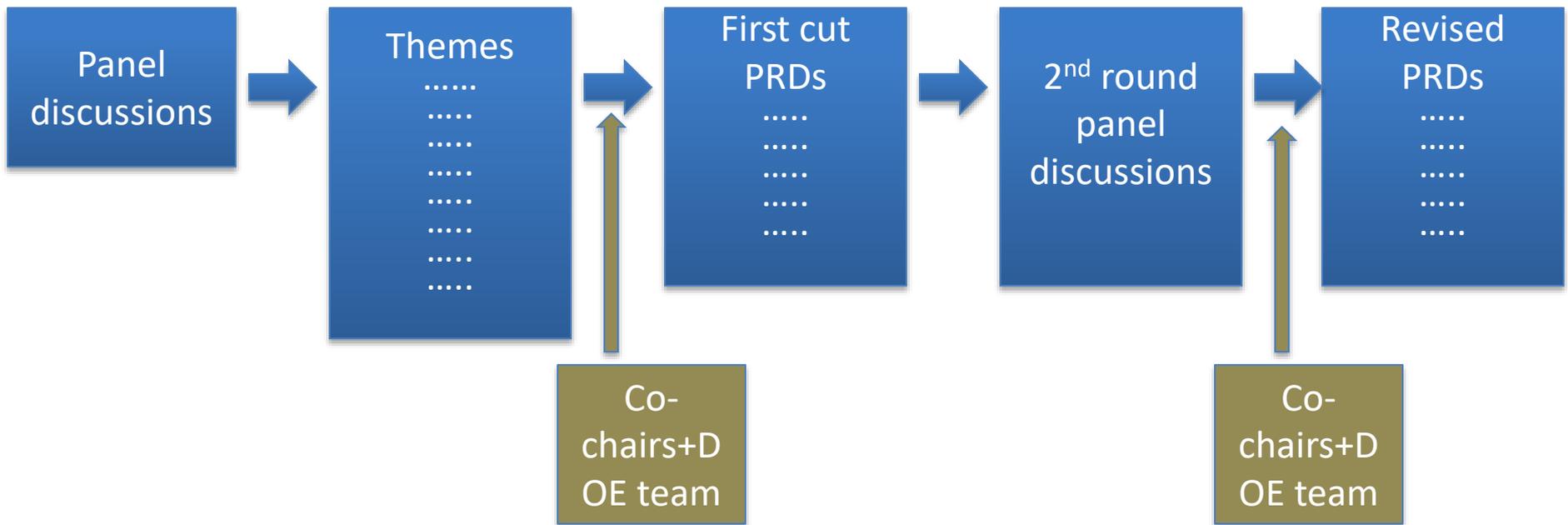
Target dates:
Brochure ready on DOE website: Dec , 2018
BRN report ready for publication: Feb 2019

Principles of co-design underpin all five priority research directions (PRDs)
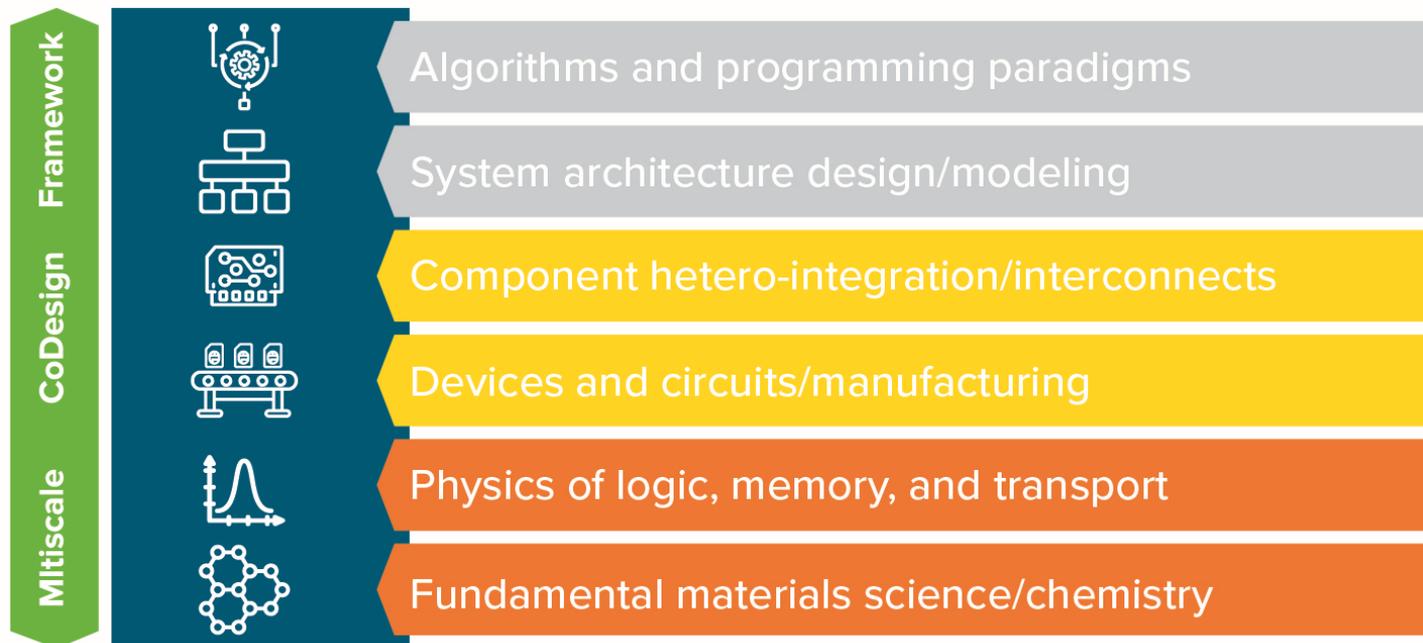
PRD 1 (DRAFT): Flip the current paradigm: Define innovative materials, device, and architecture requirements driven by applications, algorithms, and software

- Develop an "end-to-end" co-design framework
- Applications ←→ Algorithms ←→ System SW ←→ System HW

Applications

Algorithms

Architecture

- *Novel Interconnect Networks*
- *Disaggregated memory*

Circuits

MESAFab

CHISEL

- *Heterogeneous Integration*
- *STT circuit Accelerators*
- *Single-electron Charge Logic*
- *Photonic Interconnect*

Devices

- *Photonics & Plasmonic devices*
- *Single Electron devices*
- *Magnetic/spin-torque RAM*

SETs

2D-materials

Materials

Ab Initio Models

Universal Charge Device Simulator

Center for Nanoscale Materials

(100 layers, see below)

Stacked PIMS B, C, D, E, F, G, H, I, J

PIMS 3D storage layers A1-A100 configuration and memory/storage

PIMS replication unit
PIMS interconnect
PIMS logic
Fast thread CPU

Heat sink

PRD 2 (DRAFT): Revolutionize memory in computing

Typical access latency in processor cycles (@ 4 GHz)

Memory System

High-Performance Disk

L1(SRAM) EDRAM DRAM   Flash   HDD

logic   tape

2^1 2^3 2^5 2^7 2^9 2^{11} 2^{13} 2^{15} 2^{17} 2^{19} 2^{21} 2^{23}

Few ns   30 micro-s   2 ms

new non-volatile solid state memories
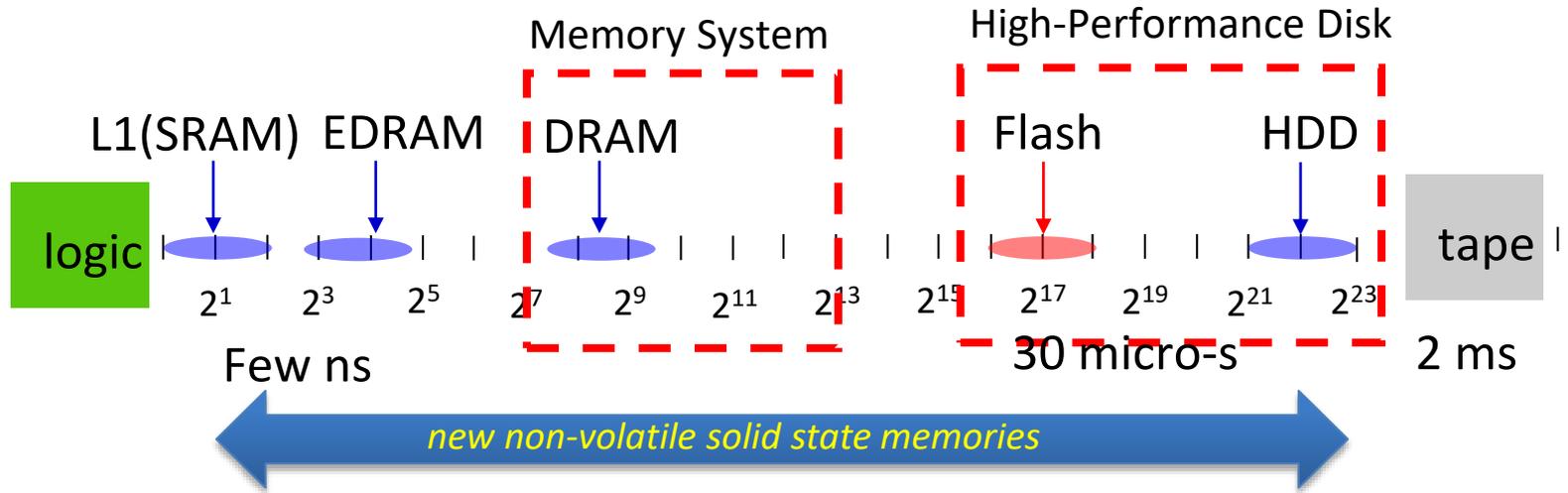
Density
Latency
Bandwidth
In-memory computing
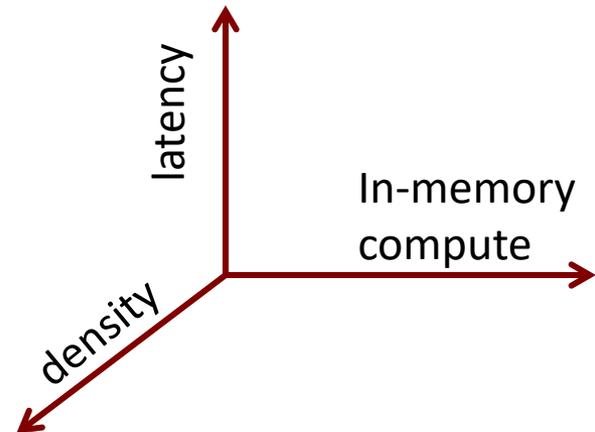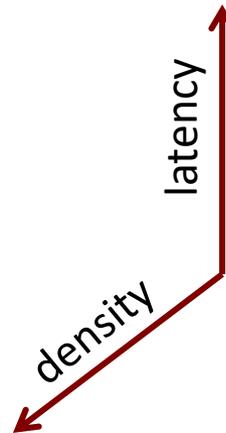
latency

density

latency

density

In-memory
compute

Data movement is growing exponentially

pJ/bit not ramping down significantly

Worthy Goal: Tbyte/sec-mm channel capacity for <100 fJ/bit
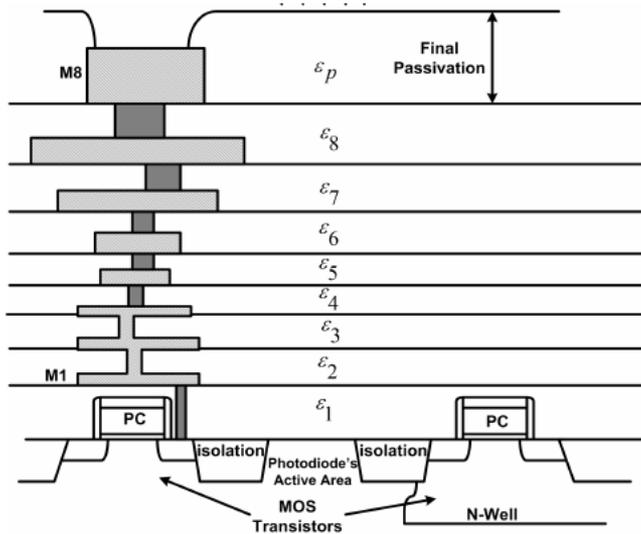
https://www.researchgate.net/figure/General-structure-of-130-nm-technology-with-Back-end-of-line-metallization-and-dielectric_fig11_224918168

https://images.anandtech.com/doci/8367/14nmInterconnect.jpg
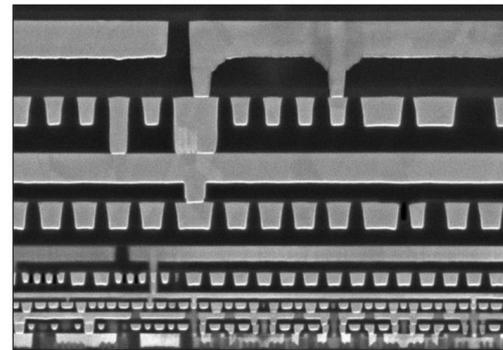
# PRD 4 (DRAFT): Redefine computing by leveraging unexploited physical phenomena

Finding and understanding physical phenomena that can express computation
New ways of reasoning about computation
Leveraging physical processes to compute ("analogous computing")
NvN Optimizers, both continuous and integer
Artificial Neural Networks
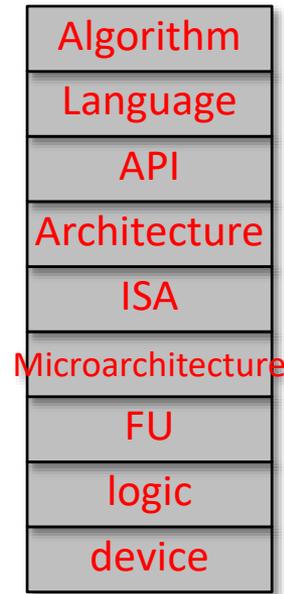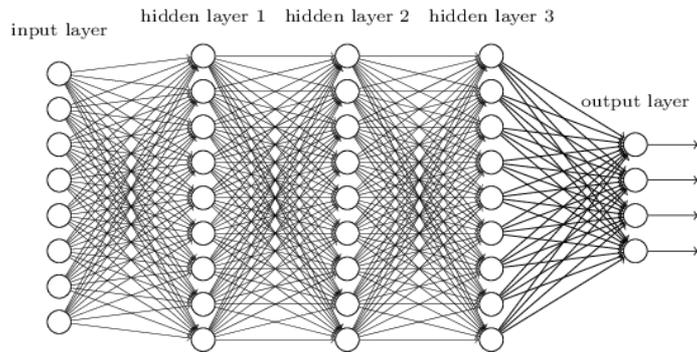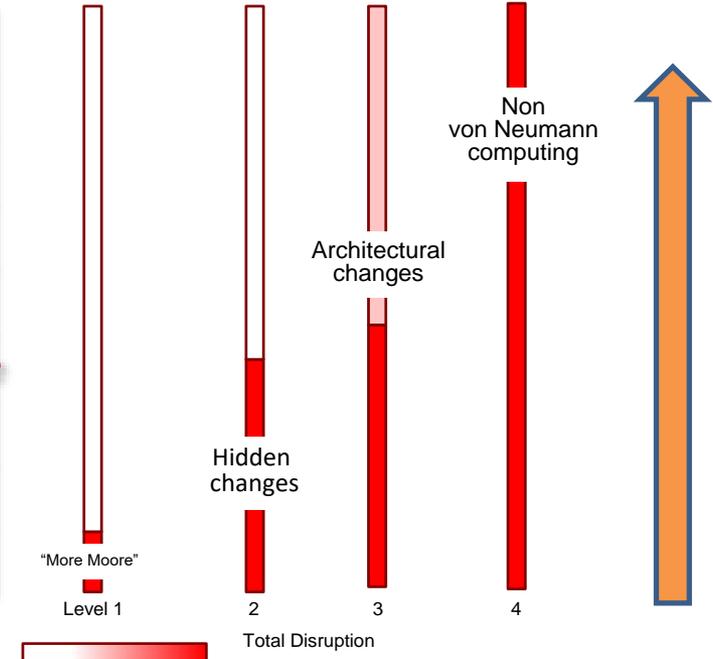
PRD 5 (DRAFT): Reinvent the electricity grid through new materials, devices, and architectures

Substation in a Suitcase

8000 lbs, 60 Hz Distribution Transformer
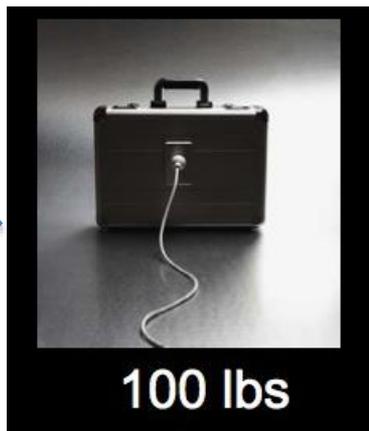
Silicon Carbide IGBT; 15 kV, 100 A; 50 kHz from Cree Inc.

100 lbs

IGBT